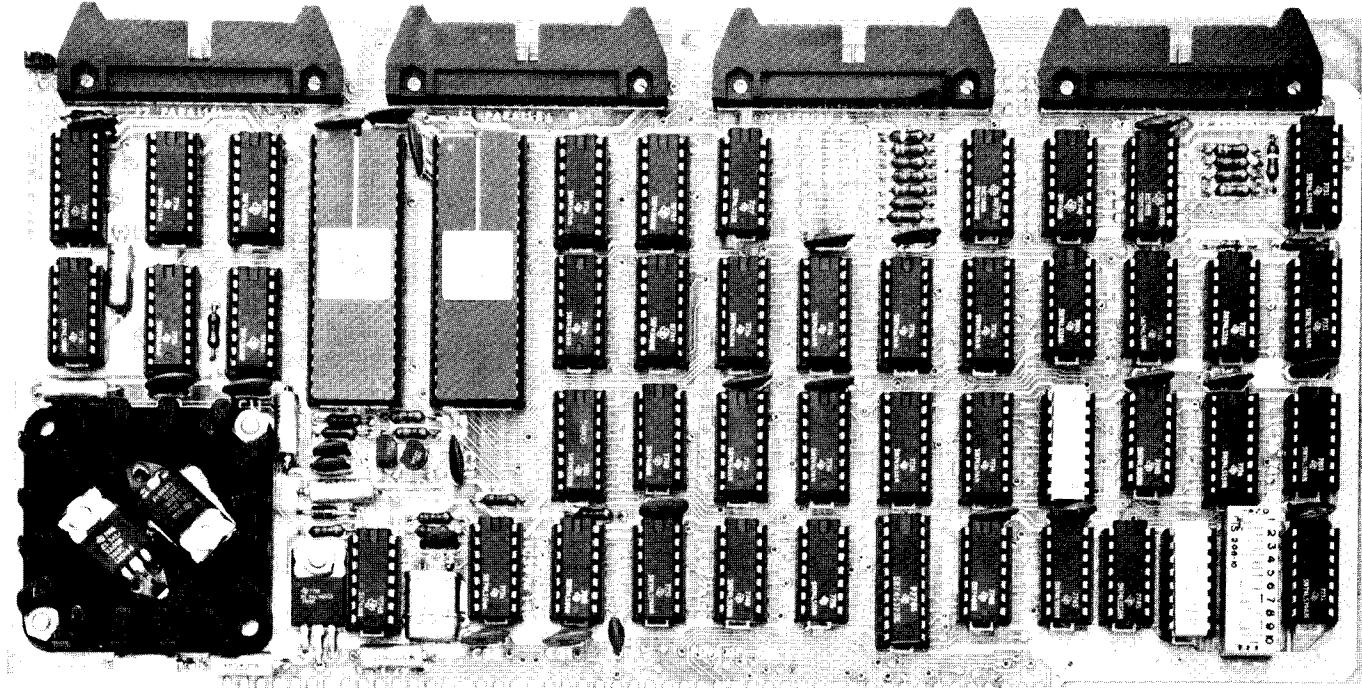


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Cromemco **TU-ART** Digital Interface



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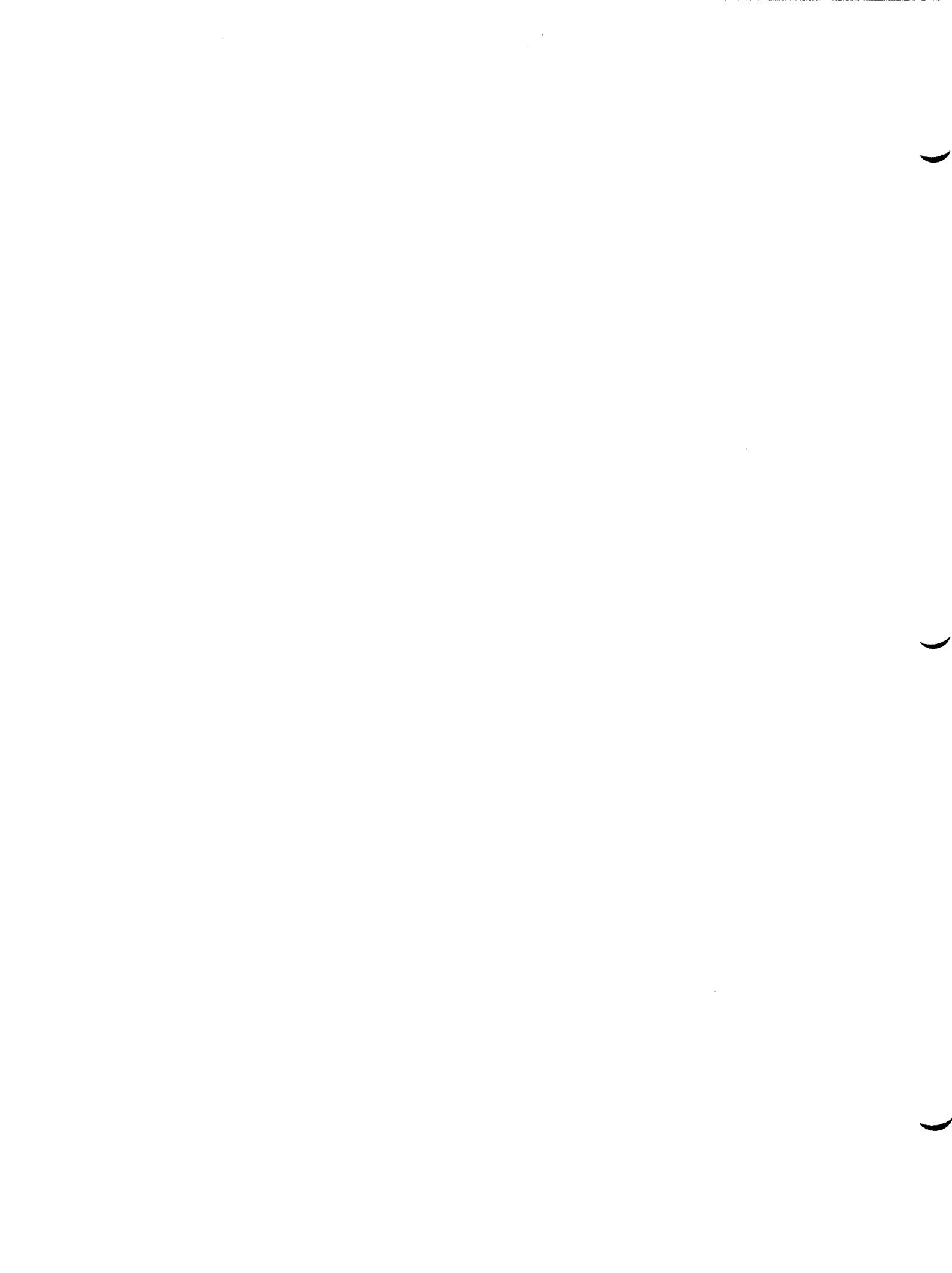


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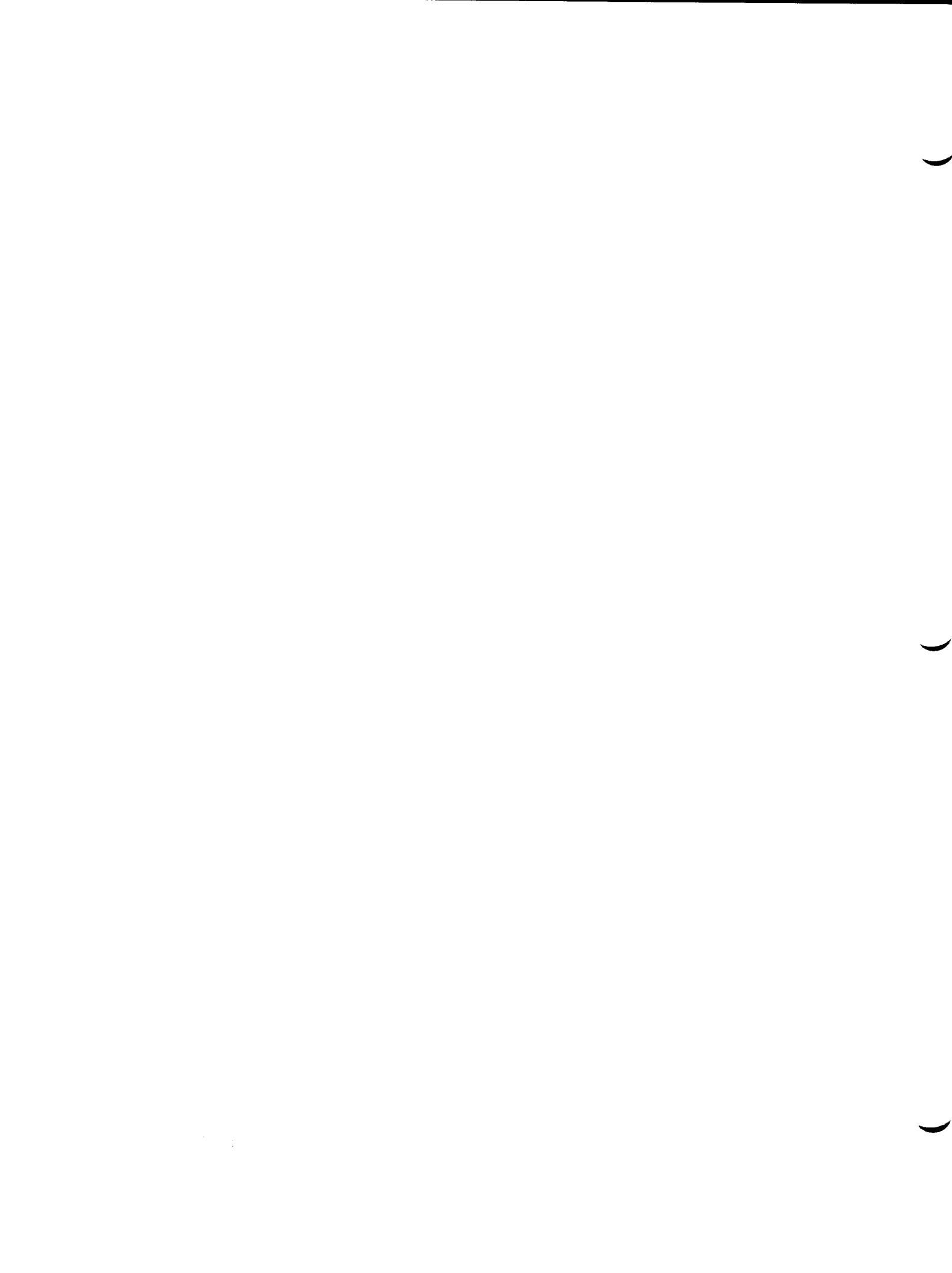


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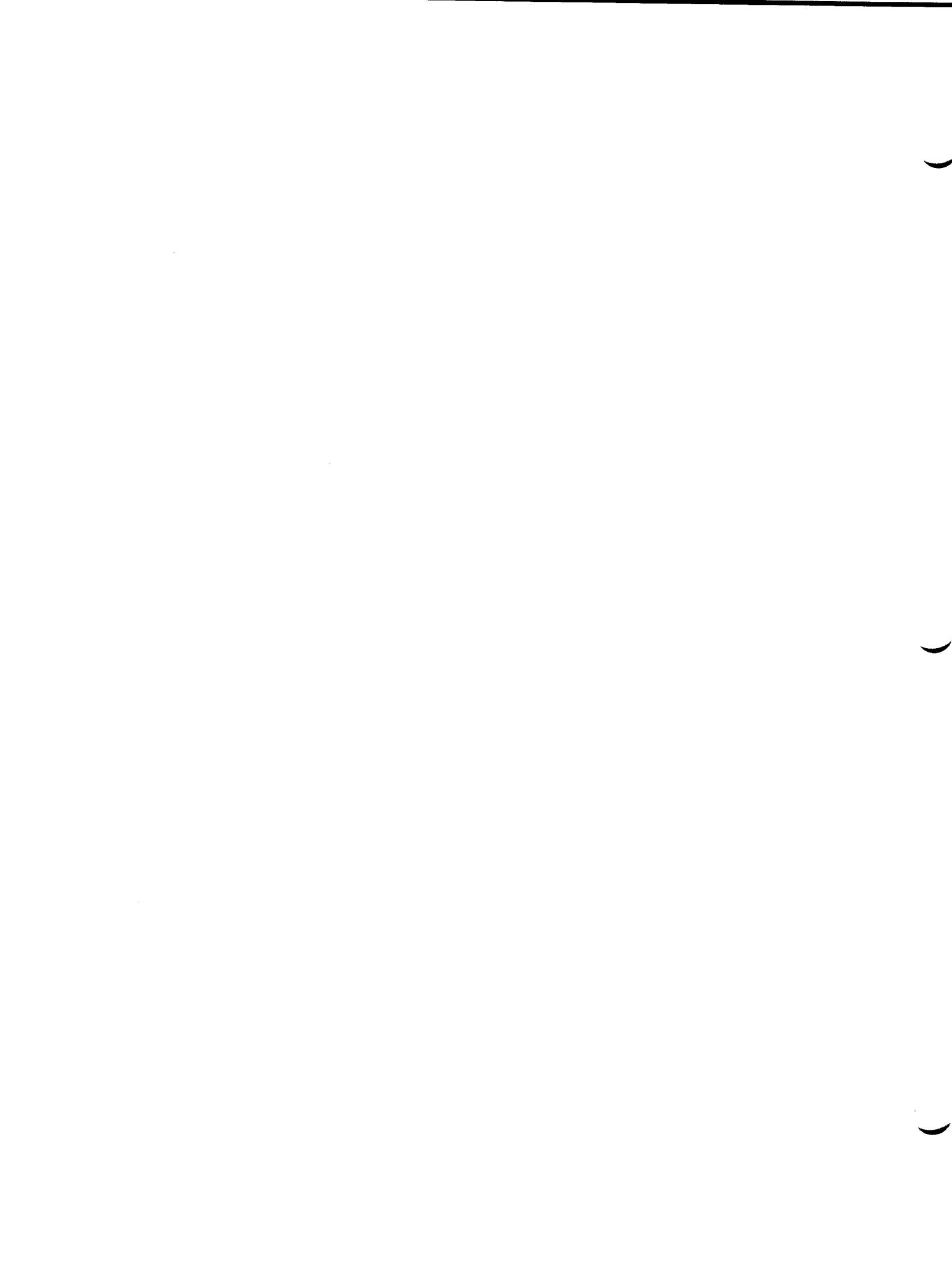
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Section 1

Introduction



Introduction

The Cromemco TU-ART (Twin Universal Asynchronous Receiver and Transmitter) provides two channels of duplex serial data exchange; two channels of parallel data exchange; and ten interval timers. Status information is available through polling or by interrupt. In addition, each interval timer activates an interrupt and two interrupt request lines are brought out for the user. The TU-ART has its own crystal-controlled clock and interfaces to the S-100 bus asynchronously so that CPU clock frequency is not critical. The TU-ART incorporates two TMS 5501 NMOS I/O Controller chips.

1.1 Definitions

Throughout this manual the two TMS 5501 chips will be referred to as "Device A" and "Device B." Device A (IC 4) is the leftmost chip. Device B (IC 5) is the rightmost chip. Device A is nearer the heat sink and drives serial connector J4 and parallel connector J2. Device B is located to the right of Device A and drives serial connector J5 and parallel connector J3.

1.2 Switch Selectable Options Addressing The TU-ART

The system CPU views the TU-ART as a dual assembly of input/output ports with interrupt capability. The CPU normally reads data or status from the TU-ART via the S-100 bus by executing an IN A, (port) instruction, and writes data or commands to the TU-ART by executing an OUT (port), A instruction.

There are fourteen I/O ports used for data transfers, commands and status by Device A, and another fourteen by Device B (see Figure 2). The user may independently switch select Device A and Device B I/O Base Addresses (the four most significant I/O address bits); the four least significant bits of the I/O address on the

S-100 bus then determine the offset from the selected base address.

The base address of Device A is selected by DIP switch positions 6 thru 3; the base address of Device B is selected by DIP switch positions 10 thru 7 (see Figure 1). Notice that positioning a switch ON conditions the TU-ART to respond to a logic 0 on its associated address line; an OFF switch corresponds to logic 1.

For example, if DIP switch positions 6 thru 3 are ON, and positions 10 thru 7 are OFF, then the TU-ART Device A Command Register is mapped into output port 02H, and the Device B Command Register is mapped into output port 0F2H.

Note that Device A bits A7, A6 and A5 also control D7, D6 and D5 of the TU-ART's Z-80 mode 2 Interrupt Acknowledge response vector.

Interrupt Mode

When this switch (position 1) is ON, the TU-ART operates in the 8080 interrupt mode: one of eight "Restart" instructions is gated to the data bus during an Interrupt Acknowledge cycle. Since the TU-ART can interrupt from one of 16 different sources, it is necessary to poll the devices if the TU-ART is in 8080 mode (see "Operation Using 8080 Mode Interrupts").

When switch position 1 is OFF, the TU-ART responds in Z-80 mode 2. In this mode, the TU-ART supplies a byte to the data bus during Interrupt Acknowledge that is used as the lower eight bits of a memory address. The Z-80 supplies the upper eight bits from the I register and automatically reads the corresponding memory location, as well as the next location, to find the starting location of an interrupt routine. (Refer to Section 3.1 and/or the Z-80 CPU Reference Manual, Zilog, 1977, for details.)

Normal/Reverse Address

When this switch (position 2) is ON, it allows Device A and Device B to swap base addresses by means of an output to one of the parallel ports (Software

Address-Reverse). This allows either Device A or Device B to be driven by a software driver whose port assignments are frozen in memory. Setting the switch ON connects the MSB of Device A's parallel output port to the Reverse Address control so that addresses may be flipped under software control. To flip addresses, output a byte with D7 high to Device A's parallel output port. To return to normal addressing, output a byte with D7 low to Device B's parallel output port. When switch position 2 is OFF, the Address Reverse switch is disconnected from the parallel port.

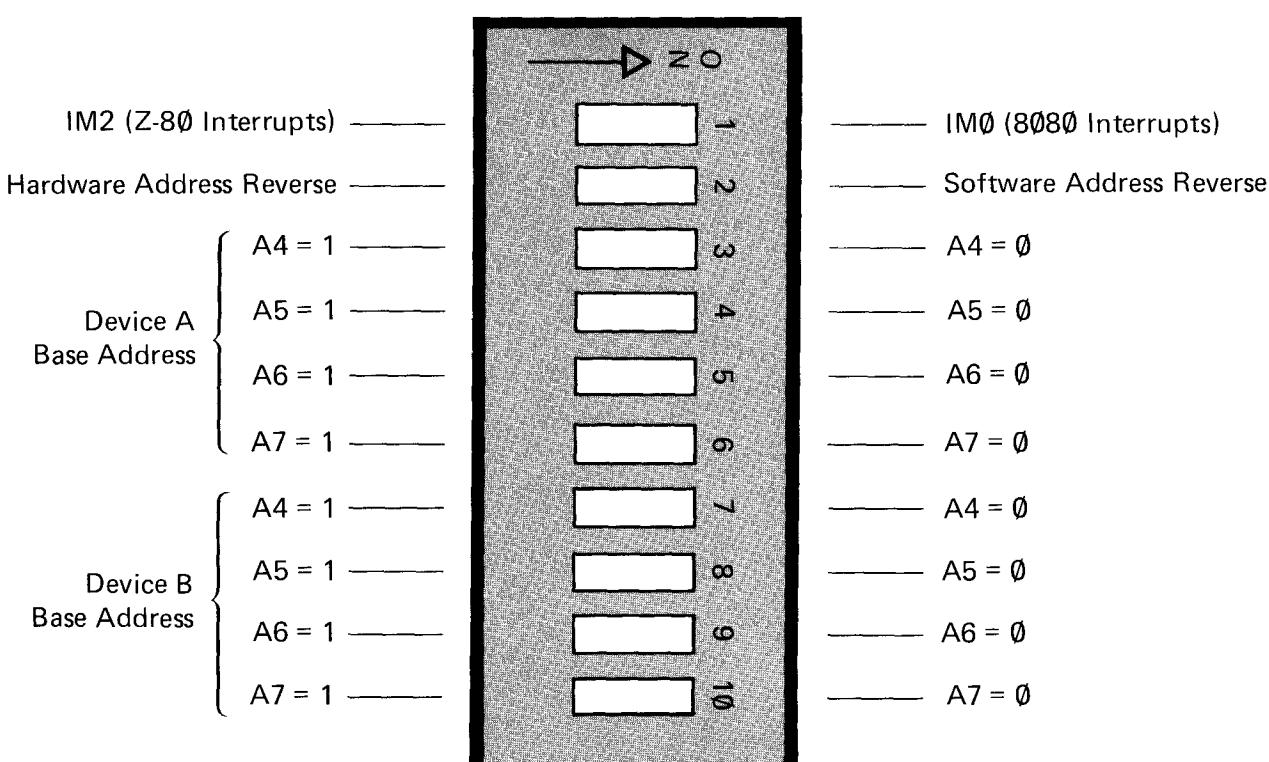
The Address Reverse signal is brought out to pin 1

of J2 and J3. When the Address Reverse switch is ON, pin 1 will show the state of the TU-ART:

Pin 1 = 0 means Reverse Mode,
Pin 1 = 1 means Normal Mode.

When the Address Reverse switch is OFF, pin 1 of J2 or J3 may be grounded externally to place the TU-ART in reverse Mode (Hardware Address-Reverse). Do not ground pin 1 of J2 or J3 while the Reverse Address switch is ON as this will conflict with operation of Device A's parallel port.

Figure 1 TU-ART Switch Settings



Caution: Base addresses 00H and 30H are used by Cromemco's 4FDC Floppy Disc Controller; 40H is used by Cromemco memory boards with BANK SE-

LECT; and 50H is used by Cromemco's PRI Printer Interface.

1.3 Interrupt Priority Chain

When more than one TU-ART is used in a system, it is necessary to coordinate the Interrupt Responses in order to prevent bus conflict during Interrupt Acknowledge cycles. This is done by first connecting J1 PRIORITY OUT from the highest priority TU-ART to J1 PRIORITY IN of the next highest priority TU-ART, then connecting J1 PRIORITY OUT of the second TU-ART to J1 PRIORITY IN of the next TU-ART, and so on until all TU-ARTs are connected. The J1 PRIORITY IN pin of the highest priority board is left unconnected. Device A is internally prioritized over Device B on each TU-ART.

If necessary, the flags may be assigned to different data bits. This may be most easily done as follows:

1. Notice that the flags are arranged along the left row of pads and that the data bits are arranged along the right side row of pads. Note also that **only** those 8 traces connecting the right and left pads are **not** covered by the solder mask. There are 5 traces which pass through this area which are covered.
2. Use a razor blade or a sharp knife to cut **all 8** of the traces connecting the left and right rows of pads. Be very careful not to cut the traces which are covered by the solder mask.
3. Install and solder a 16 pin IC socket in the 2 rows of pads.
4. Install a 16 pin "component header" in the socket.
5. Using small (24 or 28 Awg) insulated wire connect the flags (on the left) to the desired data bits (on the right) on the component header.
6. The component header is now a "plug" for your particular flag assignment. Several different flag assignment "plugs" can be prepared in the same manner and used at different times to suit the requirements of the software being executed.

Any given flag may be assigned to more than one data bit. However, each data bit can have only one flag assigned to it.

Status Socket

The status flag bits available on input port 0 are connected to the data bits by foil traces in the "status" socket located between IC's 8 and 9.

The flag assignment used by all Cromemco software is discussed in the section entitled "Register Description."

1.5 Interface Options

TTY 20 mA

To drive a Teletype, the following connections should be made (at J4 or J5 for Device A or B respectively):

TU-ART	ASR-33 TTY
J4/J5 PIN 23 connects to	Terminal strip "BL", terminal #7 (current into printer)
J4/J5 PIN 25 connects to	Terminal strip "BL", terminal #6 (return current from printer)
J4/J5 PIN 17 connects to	Terminal strip "BL", terminal #4 (current into keyboard)
J4/J5 PIN 24 connects to	Terminal strip "BL", terminal #3 (return current from keyboard)
Caution: 120 VAC is also present on terminal strip "BL" at terminals #1 and #2.	

RS/232C

An RS232 terminal (such as a CRT) may be plugged into an interface cable directly out of J4 or J5. The TU-ART assumes the role of data-set (computer) in this case. See Figure 8: Terminal to TU-ART Cable for this connection.

Parallel I/O

The parallel port output drivers may be tri-stated by grounding pin 8 of the parallel port (J2, J3). A bidirectional bus may be implemented by simply wiring the input and output lines together and using pin 8 to control the direction of data flow. Pin 8 low implies data input to the TU-ART and pin 8 high implies data output from the TU-ART.

Figure 2 Summary Of TU-ART I/O Port Addresses

OFFSET	A7 A6 A5 A4 A3 A2 A1 A0	FUNCTION
0	Device A Base Address (see Fig. 1)	IN Device A status register
0		OUT Device A baud rate register
1		IN Device A receiver data register
1		OUT Device A transmitter data register
2		OUT Device A command register
3		IN Device A interrupt address register
3		OUT Device A interrupt mask register
4		IN Device A parallel port
4		OUT Device A parallel port
5		OUT Device A timer 1
6	Device B Base Address (see Fig. 1)	OUT Device A timer 2
7		OUT Device A timer 3
8		OUT Device A timer 4
9		OUT Device A timer 5
0		IN Device B status register
0		OUT Device B baud rate register
1		IN Device B receiver data register
1		OUT Device B transmitter data register
2		OUT Device B command register
3		IN Device B interrupt address register
3		OUT Device B interrupt mask register
4		IN Device B parallel port
4		OUT Device B parallel port
5		OUT Device B timer 1
6		OUT Device B timer 2
7		OUT Device B timer 3
8		OUT Device B timer 4
9		OUT Device B timer 5

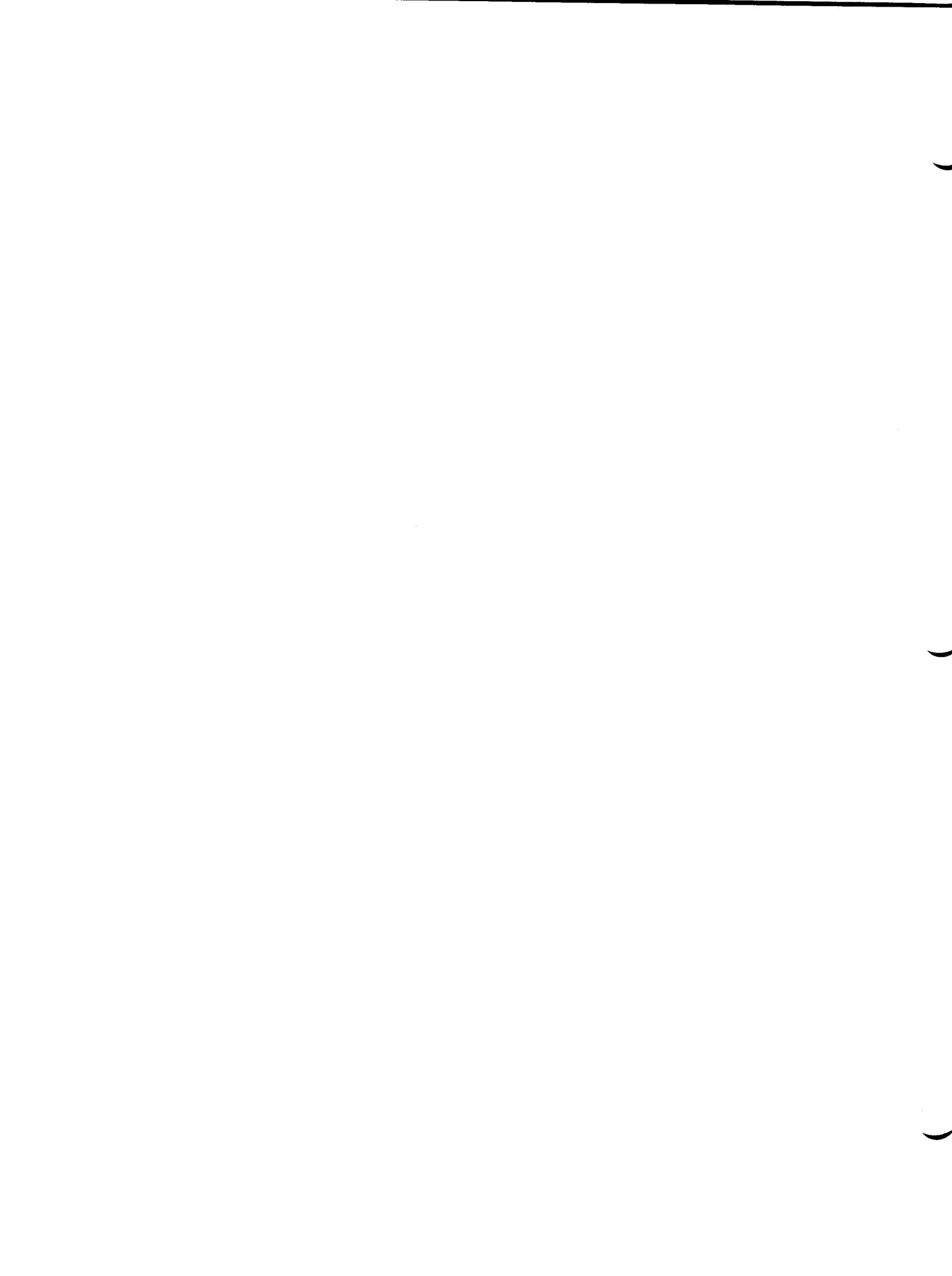
NOTES:

All of the following unassigned ports are free for system use: IN 2, IN 5 through IN 9, IN 10 through IN 15 and OUT 10 through OUT 15.

If Device A and Device B are set to the same base address, Device A will override.

Device A is IC 4.

Device B is IC 5.



Section 2

TUART Register

Descriptions

Transmit Buffer Empty	Read Data Avail.	Int. Pending	Start Bit Detect	Full Bit Detect	Serial Rcv	Over-run Error	Frame Error
-----------------------	------------------	--------------	------------------	-----------------	------------	----------------	-------------

for test purposes.

TU-ART Register Descriptions

2.1 Offset IN/OUT Description

Each of the twenty-eight TU-ART registers is viewed as an I/O port by the system CPU. The function of each register is discussed in the following subsections. The sub-section headings consist of an I/O port address offset, followed by either "IN" or "OUT," followed by the TU-ART register name. The descriptions given below apply equally to Device A registers and Device B registers. Refer to Figure 3 for a summary of TU-ART register formats.

00 IN Status Register

The CPU reads the contents of this register to determine the status of the Device A/Device B serial port. The status bit assignments may be altered by cutting PC foil traces and installing a jumper wire header (see Section 1.4).

D7	D6	D5	D4	D3	D2	D1	D0
Transmit Buffer Empty	Read Data Avail.	Int. Pend-ing	Start Bit Detect	Full Bit Detect	Ser-ial Rcv	Over-run Error	Frame Error

D7 Transmitter Buffer Empty (TBE)

A high in bit 7 indicates that the transmitter data buffer is ready to accept a new byte. TBE goes high as soon as the serial transmitter begins to send the byte currently in the buffer. Since the transmitter is "double-buffered," the user may respond to the TBE signal and load the buffer even before the previous byte has been totally transmitted. TBE also activates interrupt request 5. TBE is cleared when the buffer is loaded and is set by the RESET command.

D6 Receiver Data Available (RDA)

A high in bit 6 indicates that a byte of data is available from the receiver buffer. This flag remains high until the buffer is read. A RESET command clears the flag. If the buffer is not read by the time the next byte from the receiver is ready, the new byte will write over the old byte and the overrun error flag will be set. RDA also activates interrupt request 4.

D5 Interrupt Pending (IPG)

A high in bit 5 indicates that one or more of the eight interrupt request sources has become active. This flag goes high at the same time as the interrupt request pin of the TMS 5501.

D4 Start Bit Detect (SBD)

A high in bit 4 indicates that the serial receiver has detected a start bit. This bit remains high until the full character has been received. SBD is cleared by RESET command. This bit is provided for test purposes.

D3 Full Bit Detect (FBD)

The FBD flag in bit 3 goes high one full bit time after the start bit has been detected. This bit remains high until the full character has been received. FBD is cleared by a RESET command. This bit is provided for test purposes.

D2 Serial Receive (SRV)

A high in bit 2 indicates high level on the serial data input line. A low in bit 2 indicates a low level on the serial data input line. SRV is high when no data is being received. This bit is provided for break detection and for test purposes.

D1 Overrun Error (ORE)

A high in bit 1 indicates that the receiver has loaded the receiver data buffer before the previous contents were read. ORE is cleared after the status port is read or by the RESET command.

D0 Frame Error (FME)

A high in bit 0 indicates an error in one or both of the stop bits which "framed" the last received data byte. FME remains high until a valid character is received.

00 OUT Baud Rate Register

The CPU loads this register to set the baud rate and stop bits for serial receive and transmit data. Bit assignments are as follows:

D7	D6	D5	D4	D3	D2	D1	D0
STOP BITS	9600	4800	2400	1200	300	150	110

D7 Stop

A high in bit 7 selects one stop bit for serial receive and transmit data. A low in bit 7 selects two stop bits.

D6-D0 Baud Rate

A high in one of the lower seven bits selects the corresponding baud rate. If more than one bit is high, the highest rate selected will result. If none of the bits are high, the serial transmitter and receiver will be disabled. (For special purposes these baud rates can be octupled—see the description of HBD in the command register.)

01 IN Receiver Data

The CPU reads this register to obtain the assembled byte of data from the serial receiver.

01 OUT Transmitter Data

The CPU loads this register with a data byte for serial transmission.

02 IN Not Connected

Reading this port causes no response from the TU-ART. This input port is available to other parts of the computer system.

02 OUT Command Register

The format for the command register is as follows:

latched							
D7	D6	D5	D4	D3	D2	D1	D0
Not Used	Not Used	Test	HIGH BAUD	INTA Enable	RST7 Sel.	Break	Reset

D5 Test Bit (TB5)

A high in bit 5 disables the internal interrupt priority logic and then enables the internal clock. Thus, the signal on the INT pin of the 5501 becomes a TTL level clock of 1562.5 Hz (12.5 kHz if HBD is high—see “D4 High Baud” below). TB5 should be low for normal operation.

D4 High Baud (HBD)

A high in bit 4 octuples the rate of the internal clock. This causes the interval timers to count eight times faster and the serial data rates to increase eight-fold. When bit 4 is high, baud rates up to 76.8K baud are available for high speed data transfers.

D3 INTA Enable (INE)

A high in bit 3 allows the 5501 to respond to an Interrupt Acknowledge by gating a Restart instruction into the data bus at the correct time and resetting its internal interrupt request latch.

A low in bit 3 prevents the 5501 from detecting an INTA cycle. Bit 3 should be high for normal operation.

D2 RST7 Select (RS7)

A high in bit 2 connects the MSB of the parallel input port to the interrupt request latch for the lowest priority interrupt (interrupt 7). A low-to-high transition on the MSB of the parallel input port (PI7) will activate the interrupt request latch.

A low in bit 2 connects the output of Timer 5 to the interrupt request latch for the lowest priority interrupt (interrupt 7). When the timer count reaches zero, the interrupt request latch will be activated.

D1 Break (BRK)

A high in bit 1 holds the serial transmitter output in the low state (spacing). RES will override (see “D0 Reset” below).

A low in bit 1 allows normal operation. BRK should be low for normal operation.

D0 Reset (RES)

A high in bit 0 causes the following actions:

- a) The Serial Receiver goes into search mode;

- RDA, SBD, FBD, and ORE are set to zero. The contents of the receiver buffer are not affected.
- b) The Serial transmitter output is set high (marking). If D0 and D1 are both high, the RES function will override. RES sets TBE high.
 - c) The interrupt register is cleared except for the TBE interrupt request which is set high.
 - d) The interval timers are cleared.
- RES is not latched.

The contents of this register are logically "And"-ed with output from the interrupt request register on the 5501. A high bit in the interrupt mask allows the corresponding request to pass on into the priority encoder. A low bit in the interrupt mask inhibits the corresponding interrupt from passing any further. Since the interrupt requests are latched independently of the state of the mask, an interrupt may be requested while the mask bit is low. The request will be retained until the mask is changed and the request allowed to pass on (assuming no RES command in the interim).

03 IN Interrupt Address

The CPU reads this register to obtain the encoded address of the highest priority interrupt currently requesting service. This address is identical to the "Restart" instruction op-code for the interrupt acknowledge. Thus, the register contents may be (in order of service priority):

CONTENTS	SOURCE
C7	Timer 1
CF	Timer 2
D7	Sens
DF	Timer 3
E7	Receiver Data Available
EF	Transmitter Buffer Supply
F7	Timer 4
FF	Timer 5 or PI7

This register is provided for servicing interrupts via polling. After the register is read, the corresponding bit in the interrupt request register is reset. If the register is read when no interrupt is pending, it will read 0FFH.

03 OUT Interrupt Mask

D7	D6	D5	D4	D3	D2	D1	D0
Timer5 /PI7	Timer4	TBE	RDA	Timer3	Sens	Timer2	Timer1

04 IN Parallel Input

This register contains the data presented at J2 (Device A) or at J3 (Device B). The input data must be stable 75 ns after Input Strobe goes low. The peripheral supplying data to the TU-ART can indicate data available by activating the SENS line (or by raising the MSB of the parallel input if the RS7 bit in the command register is high).

When using Z-80 block input commands, it is not necessary to supply data at full speed. The input peripheral should simply pull down the WAIT line (pin 21 of J1 or J3) whenever Input Strobe goes low and should not let WAIT go high until the next byte is presented to the TU-ART. (The TU-ART will not read this byte until Input Strobe goes low again.)

04 OUT Parallel Output

This register contains the data which drives the parallel output buffers. The output data is guaranteed stable 1.45 μ sec after the falling edge of Output Strobe. The TTL output buffers which drive J2 (Device A) and J3 (Device B) may be put in a high-impedance state by pulling down on Disable (pin 8).

When using the Z-80 block output commands, it is not necessary to receive data at full speed. The output peripheral should simply pull down the WAIT line (pin 21 of J2 or J3) whenever Output Strobe goes low and not let WAIT go high until the output peripheral has had time to "digest" the data.

05 IN Not Connected

Same as Input 02.

05 OUT Timer 1

The CPU outputs a "count" to this register to start Timer 1. This count is decremented by 1 every 64 μ seconds after initial loading. When the count reaches zero, bit 0 of the interrupt request register is set and the timer disabled. Since the maximum count is 255, the longest interval is $255 \times 64 \mu\text{sec.} = 16.32 \text{ msec}$. Accuracy is plus 0 and minus 64 μsec . Loading a count of zero causes an immediate interrupt request to the interrupt request register. Loading a new count while the timer is counting re-initializes the timer without an interrupt request. If HBD is high in the command register, the timers will count 8 times as fast.

06 IN Not Connected

Same as Input 02.

06 OUT Timer 2

Operates in the same fashion as Timer 1.

07 IN Not Connected

Same as Input 02.

07 OUT Timer 3

Operates in the same fashion as Timer 1.

08 IN Not Connected

Same as Input 02.

08 OUT Timer 4

Operates in the same fashion as Timer 1.

09 IN Not Connected

Same as Input 02.

09 OUT Timer 5

Operates in the same fashion as Timer 1.

0AH-0FFH IN And OUT Not Connected

Addressing these I/O ports causes no response from the TU-ART. These I/O ports are available to other parts of the computer system.

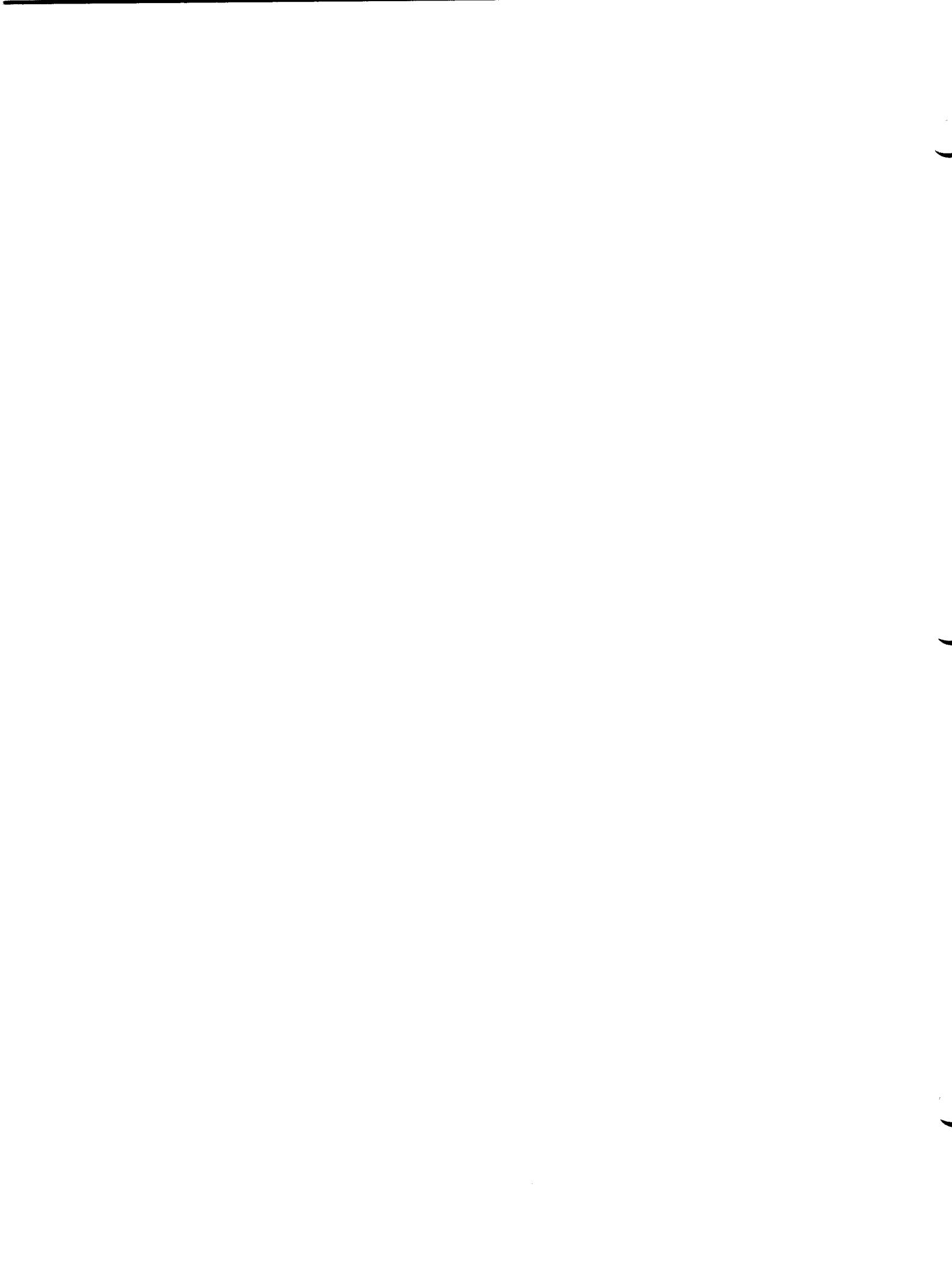
Figure 3 Summary Of Register Formats For TU-ART, Each Device

OFFSET	FUNCTION	D7	D6	D5	D4	D3	D2	D1	D0	REF. PAGE
0	IN STATUS	TBE	RDA	IPG	SBD	FBD	SRV	ORE	FME	6
0	OUT STATUS	STOP	9600	4800	2400	1200	300	150	110	7
1	IN SERIAL	MSB	Direction of shift →						LSB	7
1	OUT SERIAL	MSB	Direction of shift →						LSB	7
2	OUT COMMAND	- - -	- - -	TB5	HBD	INE	RS7	BRK	RES	7-8
3	IN INT ADDR	1	1	14*	12*	10*	1	1	1	8
3	OUT INT MASK	T5/P17	T4	TBE	RDA	T3	SENS	T2	T1	8
4	IN PARALLEL	MSB							LSB	8
4	OUT PARALLEL	MSB							LSB	8
5-9	OUT Timer 1-5	MSB	(Delay=count x 64 μsec , HBD=0) (Delay=count x 8 μsec , HBD=1)							9

*			
I4	I2	I0	Source of Interrupt
0	0	0	Timer 1
0	0	1	Timer 2
0	1	0	SENS
0	1	1	Timer 3
1	0	0	RDA
1	0	1	TBE
1	1	0	Timer 4
1	1	1	Timer 5/P17

Section 3

Interrupt Operation



Interrupt Operation

3.1 Operation Using Z80 Interrupts

The TU-ART offers sophisticated interrupt capabilities, including on-board priority encoding, interrupt generation, interrupt acknowledgment, and daisy chain expandability. These features, in conjunction with the Cromemco 4 MHz Z-80 processor, make very high throughput possible.

IMPORTANT

Both channels of the TU-ART must be properly initialized. An uninitialized TU-ART may generate spurious interrupts! Further, the rest of the system must be interrupt compatible (all Cromemco boards are, although the 8K Bytesaver requires the interrupt modification shown on the 8K Bytesaver schematic).

A description of interrupt operation follows for both the Z-80 and 8080 type interrupt modes.

When the TU-ART is used with the Cromemco ZPU, all 16 of the possible interrupt sources on the TU-ART can generate a unique response without the need for chaining the interrupt requests and polling the responses. This means fast response from interrupt request to service routine and, when coupled with the 4MHz Z-80, an extremely powerful realtime system can be implemented.

A "high priority" interrupt request is one which takes precedence over lower priority requests. This is shown in the following table where the interrupts serviced first are at the top.

It is, of course, possible to use the interrupt mask of each Device to selectively enable and disable the sources of interrupts (reference the description of OUT 03, Interrupt Mask, in the previous section). Remember that the INE bit in the status register must be high for correct operation of Interrupt Acknowledge cycles. Also, be sure that the Z-80 has executed the interrupt mode setting command 0ED5EH

Table 1 Z80 (Mode 2) Response

Priority	TU-ART's (Hex) Z-80 INTA Response									Source of Interrupt
	D7	D6	D5	D4	D3	D2	D1	D0		
15 (Highest)				0	0	0	0	0		Device A, Timer 1
14				0	0	0	1	0		Device A, Timer 2
13				0	0	1	0	0		Device A, SENSA
12				0	0	1	1	0		Device A, Timer 3
11				0	1	0	0	0		Device A, RDA
10				0	1	0	1	0		Device A, TBE
9				0	1	1	0	0		Device A, Timer 4
8				0	1	1	1	0		Device A, Timer 5 (PI7)
7				1	0	0	0	0		Device B, Timer 1
6				1	0	0	1	0		Device B, Timer 2
5				1	0	1	0	0		Device B, SENSB
4				1	0	1	1	0		Device B, Timer 3
3				1	1	0	0	0		Device B, RDA
2				1	1	0	1	0		Device B, TBE
1				1	1	1	0	0		Device B, Timer 4
0 (Lowest)				1	1	1	1	0		Device B, Timer 5 (PI7)

("IM2") and the interrupt enable command $\$FBH$ ("EI"). Both of these instructions must be executed each time the Z-80 is RESET.

Assuming that both the Z-80 and the TU-ART have been initialized, the reception of a byte of serial data at Device B would initiate the following sequence of events:

- a) The assembled byte is loaded into the receiver data buffer.
- b) The RDA status bit is set and the interrupt request register (bit 3) is set.
- c) If bit 3 of the interrupt mask of the Device in question is a one, the request passes on to the priority encoder. If bit 3 is a zero, no further action occurs until the mask is changed.
- d) The priority encoder compares all incoming interrupt requests and sets its output to the value of the highest priority incoming interrupt. Thus, since Device B receives the serial data byte in our example; the priority encoder will set its output to "priority 3" if Timers 1, 2, 3, and \overline{SENSB} from Device B are inactive or masked out.
- e) Device B's INT pin goes high, which in turn pulls \overline{PINT} low on the S-100 bus.
- f) The Z-80 checks the interrupt line at the end of the current instruction, and finding the line active, goes into an Interrupt Acknowledge (INTA) cycle.
- g) The occurrence of the INTA cycle is detected by the TU-ART which then transmits PRIORI-

TY OUT = \emptyset to connector J1. This temporarily disables Interrupt Acknowledge from lower priority boards. If no board with higher priority is holding PRIORITY IN low, and if Device A has no interrupt pending, then Device B gates the proper Z-80 INTA response vector onto the data bus. In this example, Device B would place 18H logically ORed with (A7) (A6) (A5) $\$0000$ from Device A's base address on the data bus. The corresponding bit in the interrupt request latch is reset.

- h) The Z-80 reads the INTA response byte and appends it to the byte in the I register. This then forms a sixteen bit address which points to the first of two sequential bytes in memory which in turn designate the actual starting address of the service routine. The CPU automatically executes a CALL to this starting address.

3.2 Operation Using 8080 Mode Interrupts

When the TU-ART is used in Z-80 interrupt mode 0 it is necessary to "chain" Device B through the SENS input on Device A. This requires one of the eight INTA responses, RST2 $\$D7H$, to be serviced by a routine which polls the status and interrupt address registers of Device B. The remaining seven INTA responses are serviced immediately. The resulting priority assignments are shown in Table 2.

Table 2 Z80 (Mode 0) Response

Priority	TU-ART's (Hex) 8080 INTA Response	Source of Interrupt
15 (Highest)	C7 (RST0)	Device A, Timer 1
14	CF (RST1)	Device A, Timer 2
13	D7 (RST2)	Device B, Timer 1
12	D7 (RST2)	Device B, Timer 2
11	D7 (RST2)	Device B, \overline{SENSB}
10	D7 (RST2)	Device B, Timer 3
9	D7 (RST2)	Device B, RDA
8	D7 (RST2)	Device B, TBE
7	D7 (RST2)	Device B, Timer 4
6	D7 (RST2)	Device B, Timer 5 (PI7)
5	D7 (RST2)	Device B, \overline{SENSA}
4	DF (RST3)	Device A, Timer 3
3	E7 (RST4)	Device A, RDA
2	EF (RST5)	Device A, TBE
1	F7 (RST6)	Device A, Timer 4
0 (Lowest)	FF (RST7)	Device A, Timer 5 (PI7)

It is of course, possible to use, the interrupt mask of each Device to selectively enable and disable the sources of interrupts (reference the discussion of OUT 03, Interrupt Mask, in the previous section).

It is not necessary to reset the INE status bit of Device B to zero even though Device B can never respond directly to an Interrupt Acknowledge (INTA) cycle. The INTA status information is not fed to Device B if 8080 mode INTA has been selected on the Option DIP Switch. Therefore, the 5501 never attempts to drive the bus during INTA.

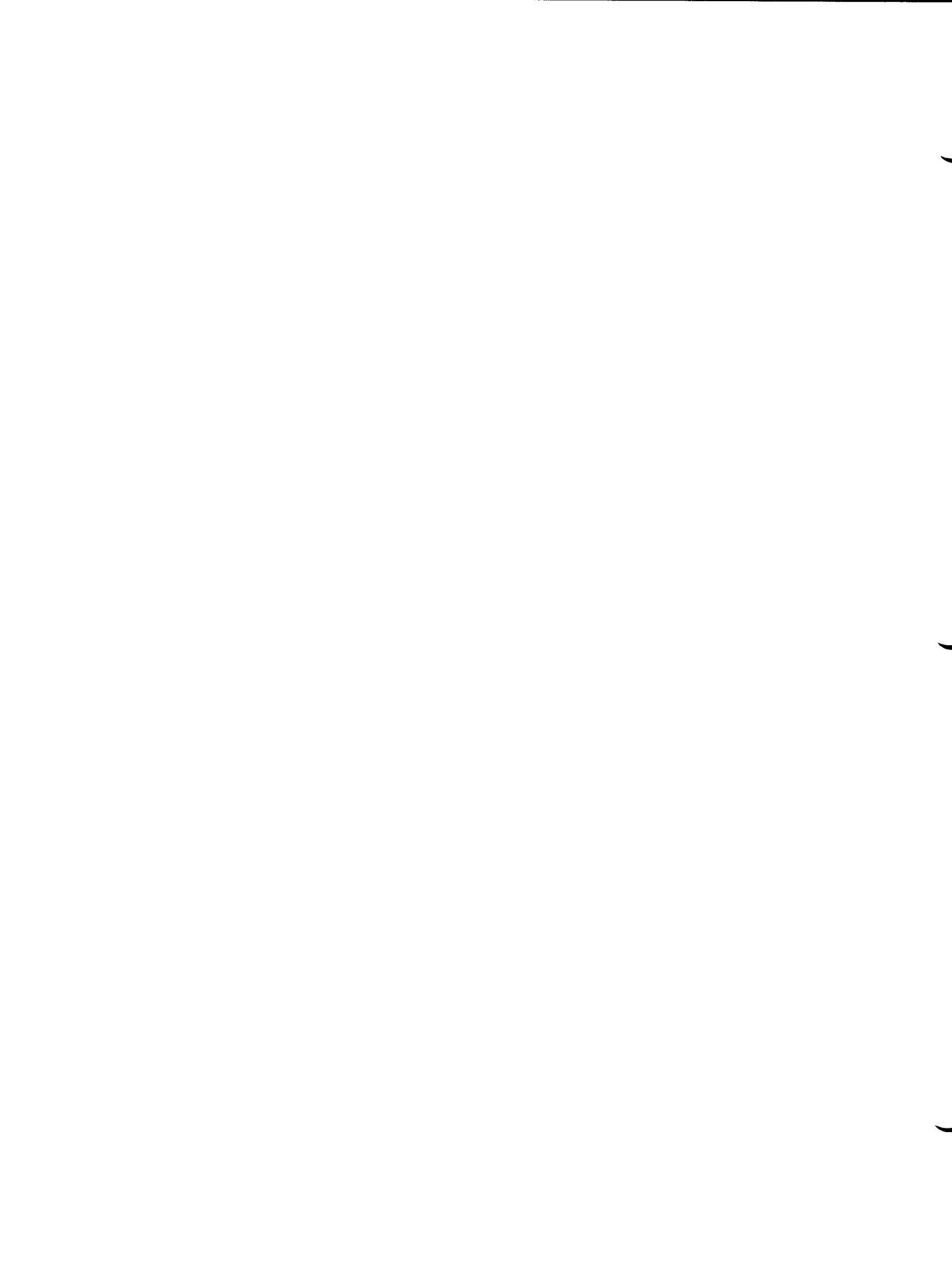
No wiring changes are necessary to disconnect the INT pin of Device B from the PINT driver and to connect it to the Device A SENS pin. All this is done automatically when 8080 mode INTA has been selected on the Option DIP Switch. Note that SENSA at J1 is still connected. Pulling this line low will generate an interrupt request. The Z-80 must execute the EI instruction (0FBH) after resets or interrupts before an interrupt may take place.

The sequence of events corresponding to Device B receiving a byte of serial data are as follows:

- a) The assembled byte is loaded into the receiver data buffer.
- b) The RDA status bit is set, the interrupt request register bit 3 is set, and the IPG status bit is set in the device which received the character (Device B in this example).
- c) If bit 3 of the interrupt mask of the device in question is a one, the interrupt request passes on to the priority encoder. If bit 3 is a zero, no further action occurs until the mask is changed.
- d) The priority encoder compares all incoming interrupt requests and sets its output to the value of the highest priority incoming interrupt. Thus, if Device B received the serial data byte in our example, the priority encoder will set its output to priority three if and only if Device B's Timers 1, 2, and 3 and SENSB are inactive or masked out.
- e) Device B's INT pin goes high which in turn activates the SENS pin of Device A.
- f) If bit 2 of Device A's interrupt mask is a one, the interrupt request will pass on to the priority

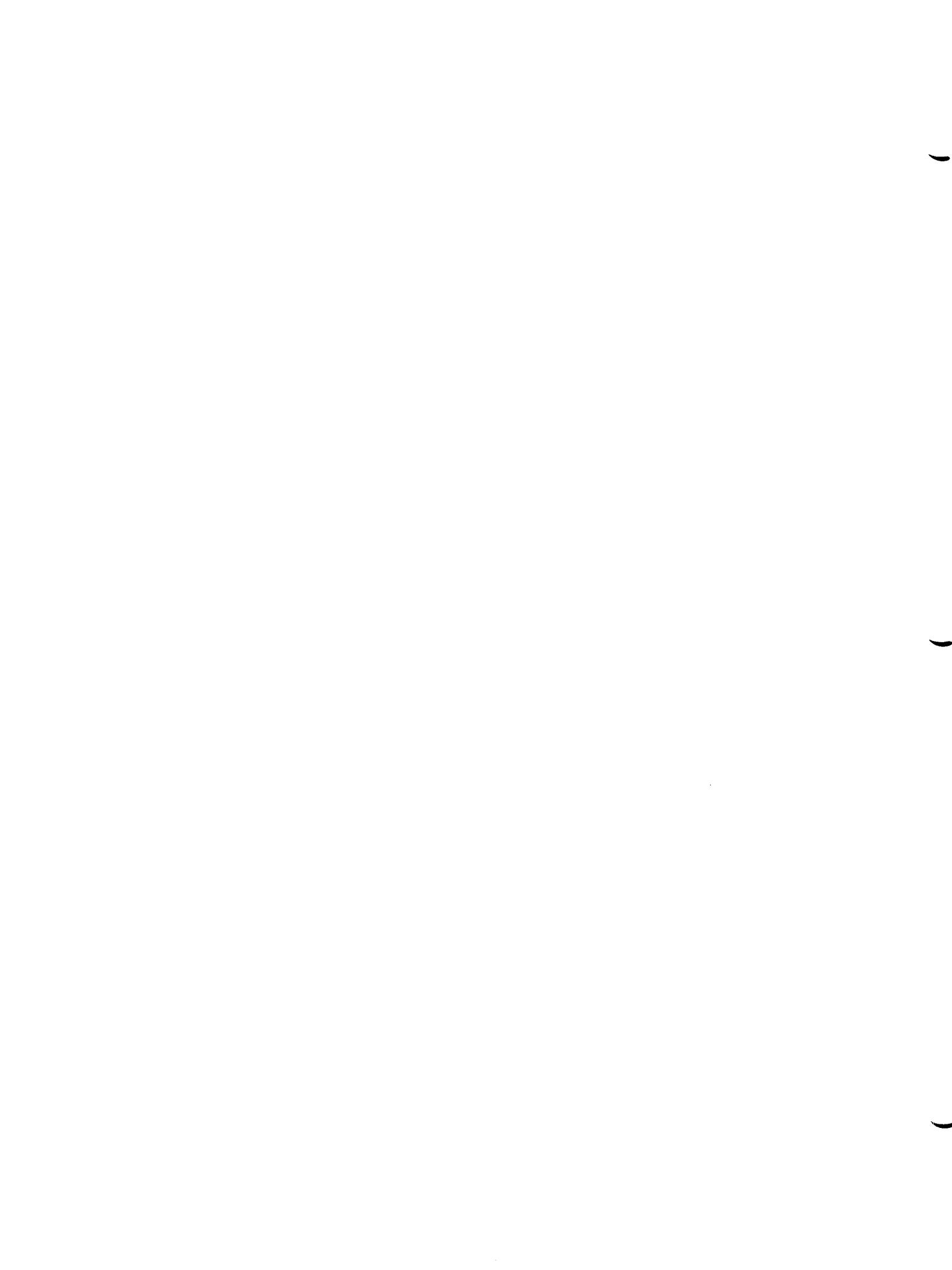
encoder. If bit 2 is a zero, no further action occurs until the mask is changed.

- g) The priority encoder in Device A compares all incoming interrupt requests and sets its output to the value of the highest priority incoming interrupt. In our example, the interrupt from Device B activates the SENS input at Device A. This interrupt will have top priority if and only if Device A's Timers 1 and 2 are inactive or masked out.
- h) Device A's INT pin goes high which in turn pulls PINT low on the S-100 bus.
- i) The CPU checks the interrupt line at the end of the current instruction and, finding it active, goes into an Interrupt Acknowledge (INTA) cycle.
- j) The occurrence of the INTA cycle is detected by the TU-ART which then transmits PRIORITY OUT = 0 to J1. This temporarily disables Interrupt Acknowledge from lower priority boards. If no board with high priority is holding PRIORITY IN low, Device A will gate an 8080 INTA response onto the bus. In this example, Device A would place 0D7H on the data bus (RST2). The corresponding bit in Device A's interrupt request register is reset.
- k) The Z-80 reads the INTA response byte and performs a CALL to location 10H, the starting address of the RST2 service routine.
- l) The service routine located at starting location 10H, reads the status register of Device B. If IPG is zero, no interrupts are pending in Device B so that the interrupt request must have originated from the SENSA line. The service routine branches to the appropriate subroutine. If IPG is one, Device B has an interrupt pending which must be serviced. The source of the interrupt is determined by reading Device B's Interrupt Address register. In our example, the Interrupt Address register would contain E7H. When this byte is read, the corresponding bit of the interrupt request register will be reset. The service routine has now determined the true cause of the interrupt and branches to the appropriate subroutine.



Section 4

Connecting The TUAART to I/O Devices



Connecting The TU-ART To I/O Devices

4.1 Parallel Ports

Each device has an 8-bit output port and an 8-bit input port with TTL buffering. The I/O connectors J2 and J3 provide these signals, along with several control lines. A full listing of these lines and their pin assignments is given in Tables 3 and 4.

Figure 4 shows the timing of the TU-ART's parallel ports. Notice that the CPU driven Input Strobe (ISB) line is low while the TU-ART is reading the parallel port. Data should become stable no later than 75 nanoseconds after ISB goes low and should be held stable for at least 40 nanoseconds after ISB goes high.

The CPU driven Output Strobe (OSB) line goes low while the TU-ART is loading a byte from the S-100 bus. There is an additional delay of up to 450 nanoseconds inside the TMS 5501 IC, so data becomes available at J2 or J3 a maximum of 450 nanoseconds after OSB goes high.

Figures 5 and 6 show suggested circuits for block-mode transfers. In these schemes, the peripheral requests service from the processor and holds down the "ready" (Wait) lines between bytes.

Figure 4 Parallel Port Timing

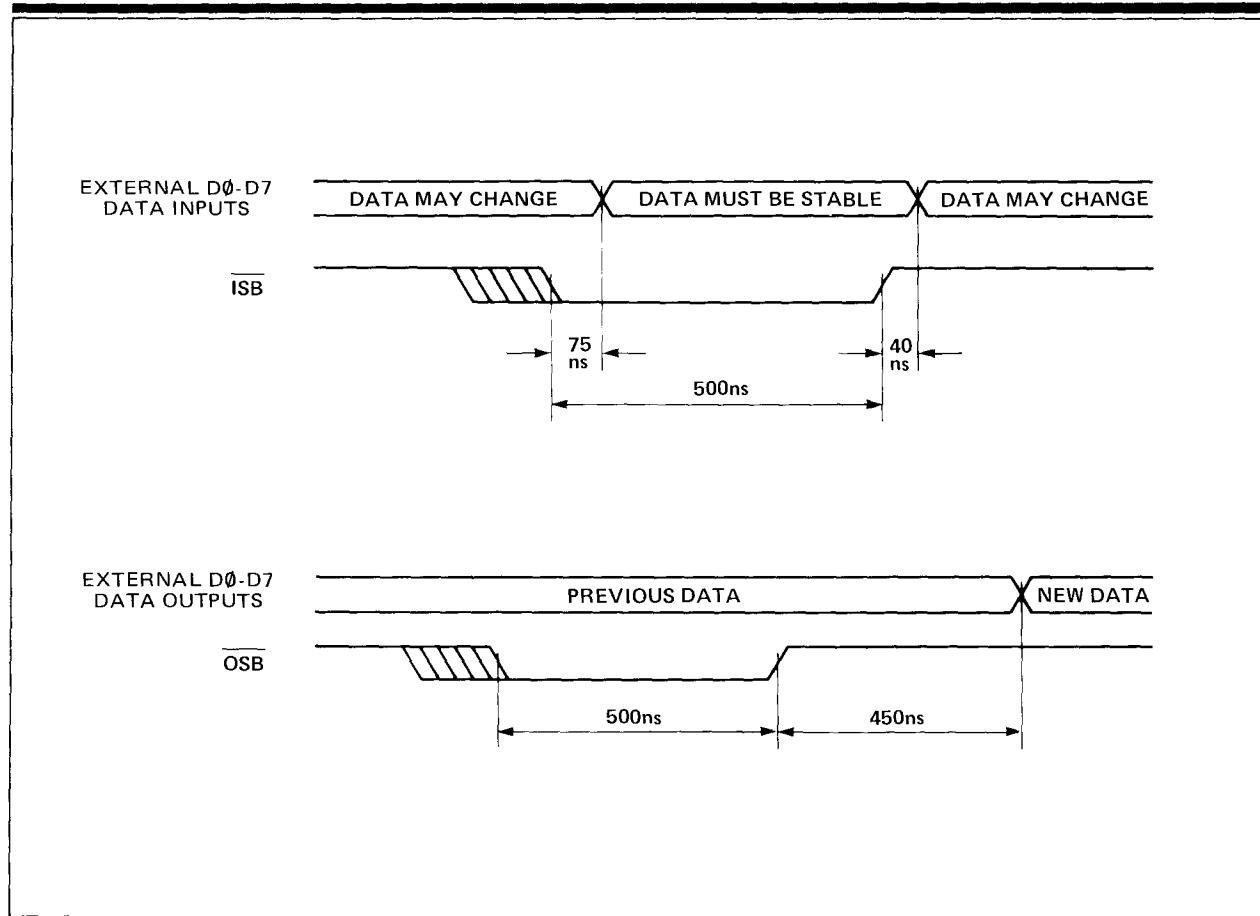


Figure 5 Suggested Block Input Circuit

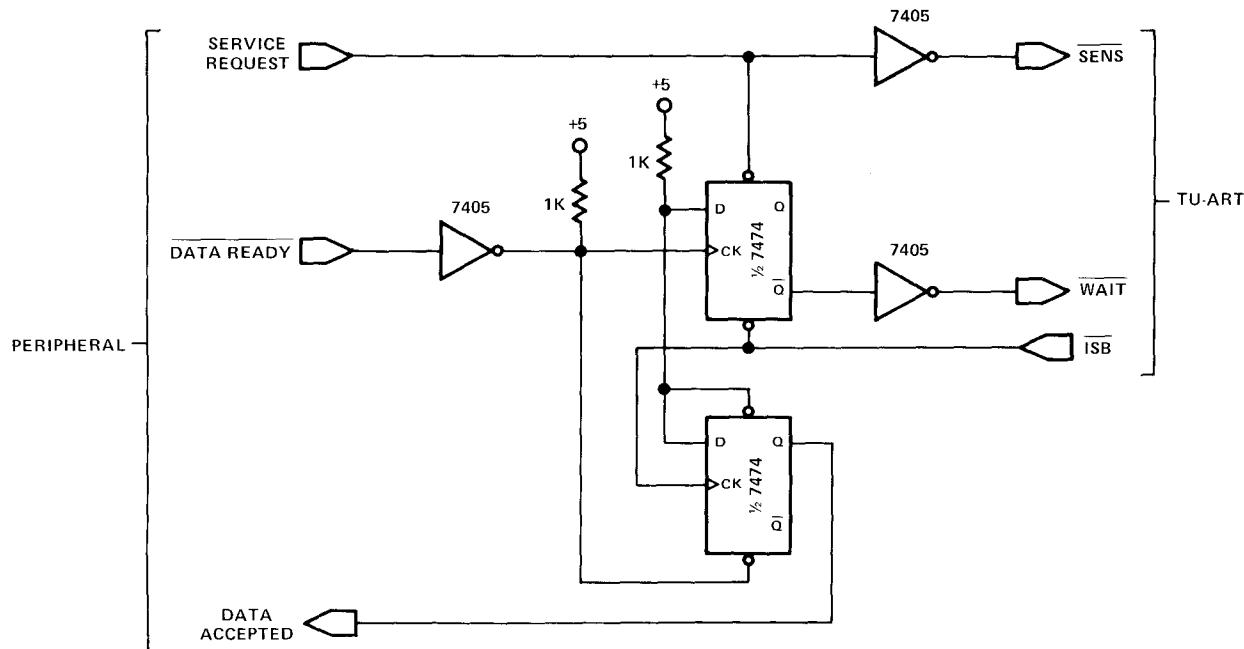
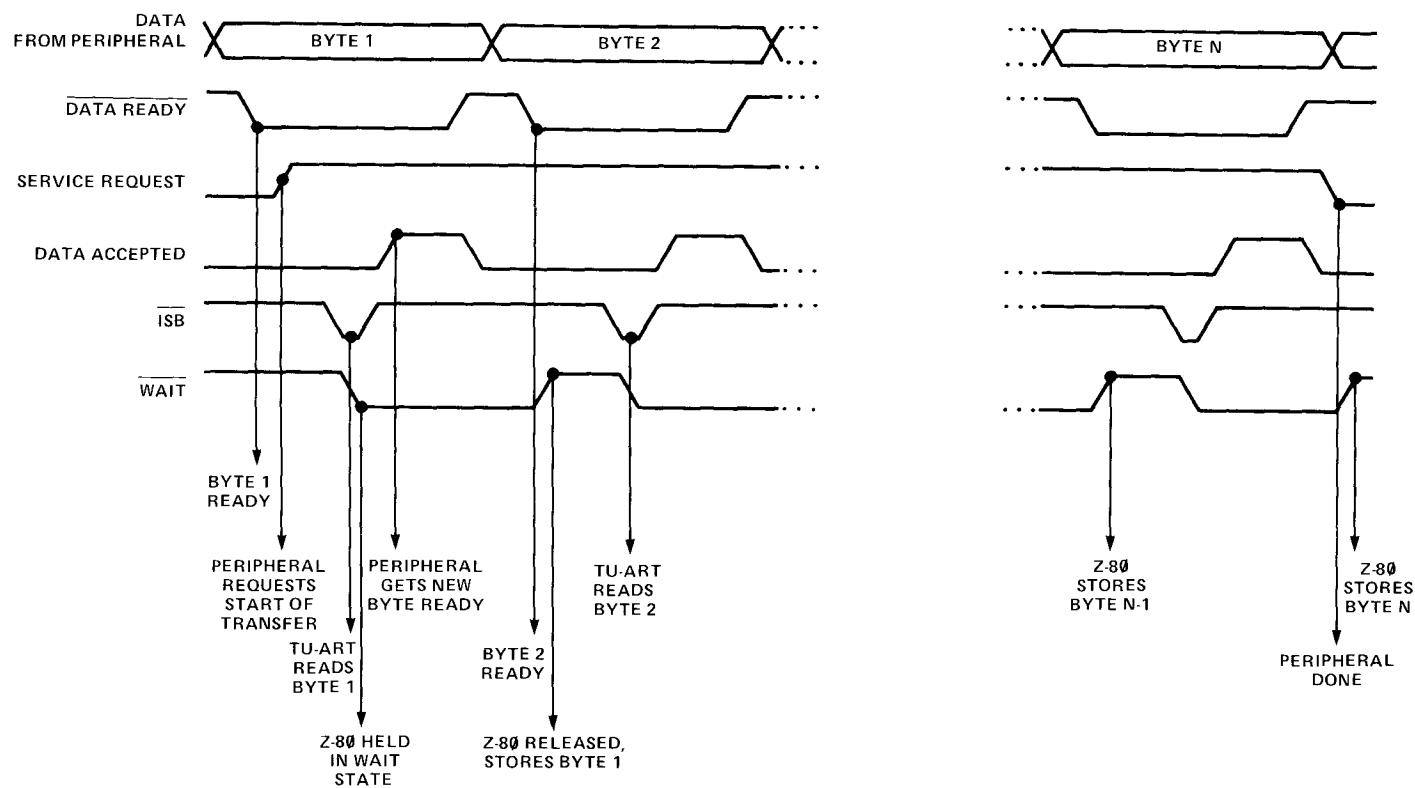


Figure 6 Suggested Block Output Circuit

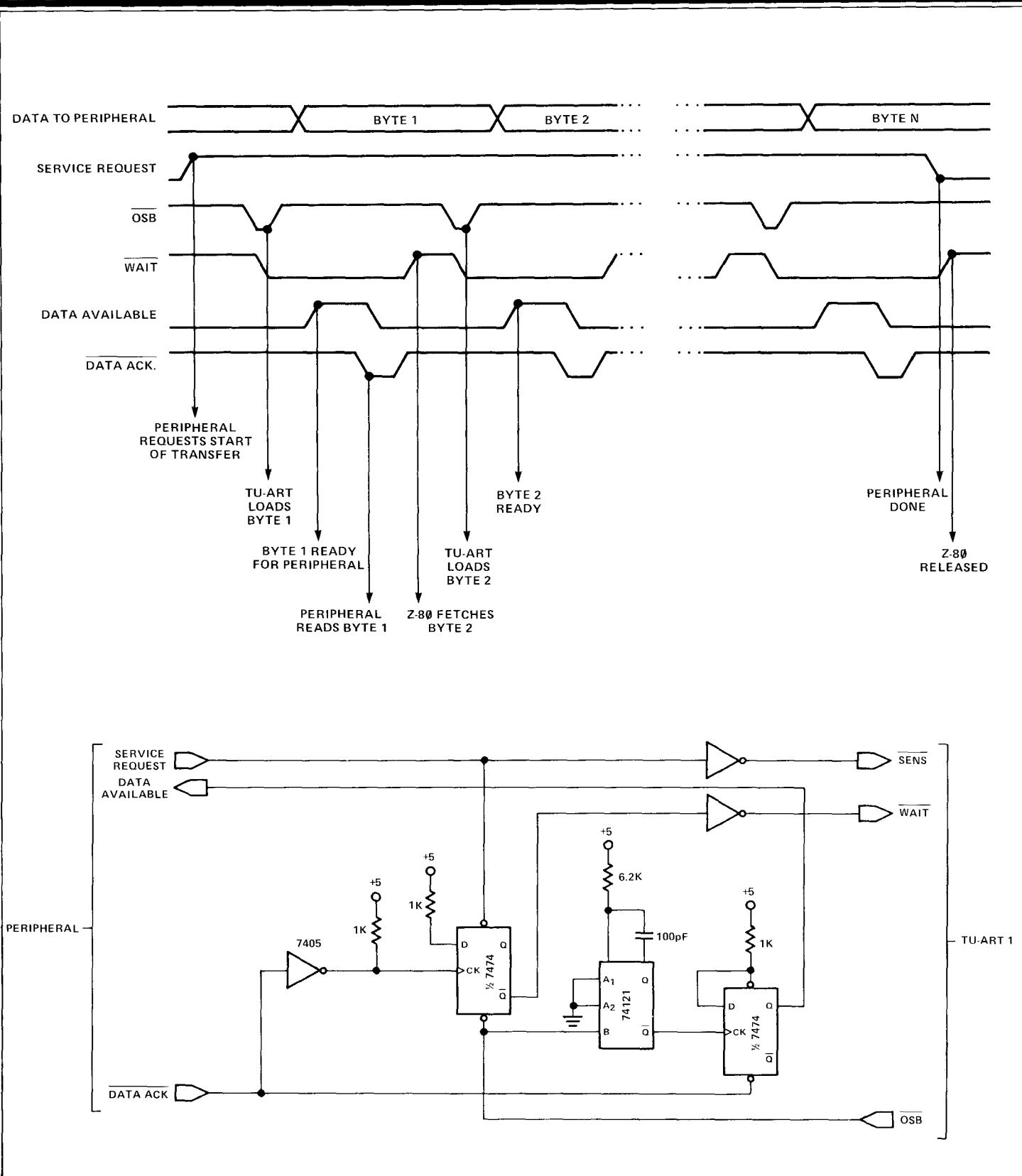


Table 3 J2 Parallel A

Pin	Name	Signal Direction	Voltage Level	Function
1	Invert	Input	TTL	Used for normal/reverse address switching. See discussion under "Switch Selectable Options."
2	Input Strobe A	Output	TTL	When active indicates that data present on input bits 0 -7 is being sampled.
3	Vcc	Output	+5V	
4	Bit 6	Input	TTL	
5	Bit 4	Input	TTL	
6	Bit 2	Input	TTL	
7	Bit 0	Input	TTL	
8	Disable	Input	TTL	Turns the output drivers for the parallel output bits OFF.
9	Output Strobe A	Output	TTL	Indicates that data is present on parallel output bits 0-7.
10	Bit 6	Output	TTL	
11	Bit 4	Output	TTL	
12	Bit 2	Output	TTL	
13	Bit 0	Output	TTL	
14	Signal Ground	Output	0V	
15	SENS A	Input	TTL	Interrupt request, input to IC 4 5501 (A)
16	Bit 7	Input	TTL	
17	Bit 5	Input	TTL	
18	Bit 3	Input	TTL	
19	Bit 1	Input	TTL	
20	NMI	Input	TTL	Non maskable interrupt. This pin is tied directly to pin 12 of the S-100 bus. Consult the Z-80 manual for use. Only usable with the Cromemco ZPU card.
21	Wait	Input	TTL	This pin is tied directly to pin 72 (PRDY) of the S-100 bus. Forces the CPU to wait when held low.
22	Bit 7	Output	TTL	
23	Bit 5	Output	TTL	
24	Bit 3	Output	TTL	
25	Bit 1	Output	TTL	

Table 4 J3 Parallel B

Pin	Name	Signal Direction	Voltage Level	Function
1	Invert	Input	TTL	Used for normal/reverse address switching. See discussion under "Switch Selectable Options."
2	<u>Input Strobe B</u>	Output	TTL	When active indicates that data present on input bits 0-7 is being sampled.
3	Vcc	Output	+5V	
4	Bit 6	Input	TTL	
5	Bit 4	Input	TTL	
6	Bit 2	Input	TTL	
7	Bit 0	Input	TTL	
8	<u>Disable</u>	Input	TTL	Turns the output drivers for the parallel output bits OFF.
9	<u>Output Strobe B</u>	Output	TTL	Indicates that data is present on parallel output bits 0-7.
10	Bit 6	Output	TTL	
11	Bit 4	Output	TTL	
12	Bit 2	Output	TTL	
13	Bit 0	Output	TTL	
14	<u>Signal Ground</u>	Output	0V	
15	<u>SENS B</u>	Input	TTL	Interrupt request, input to IC 5501 (B).
16	Bit 7	Input	TTL	
17	Bit 5	Input	TTL	
18	Bit 3	Input	TTL	
19	Bit 1	Input	TTL	
20	<u>PRESET</u>	Input	TTL	Preset. This pin is tied directly to pin 75 of the S-100 bus. Consult the Z-80 manual for use. Only usable with the Cromemco ZPU card.
21	<u>Wait</u>	Input	TTL	This pin is tied directly to pin 72 (PRDY) of the S-100 bus. Forces the CPU to wait when held low.
22	Bit 7	Output	TTL	
23	Bit 5	Output	TTL	
24	Bit 3	Output	TTL	
25	Bit 1	Output	TTL	

4.2 Serial Ports

Device A and Device B each have a bidirectional serial port with RS-232 and current loop buffering. The I/O connectors J4 and J5 provide access to these signal lines, along with several control lines. A full

listing of the J4 and J5 pin assignments is shown in Tables 5 and 6.

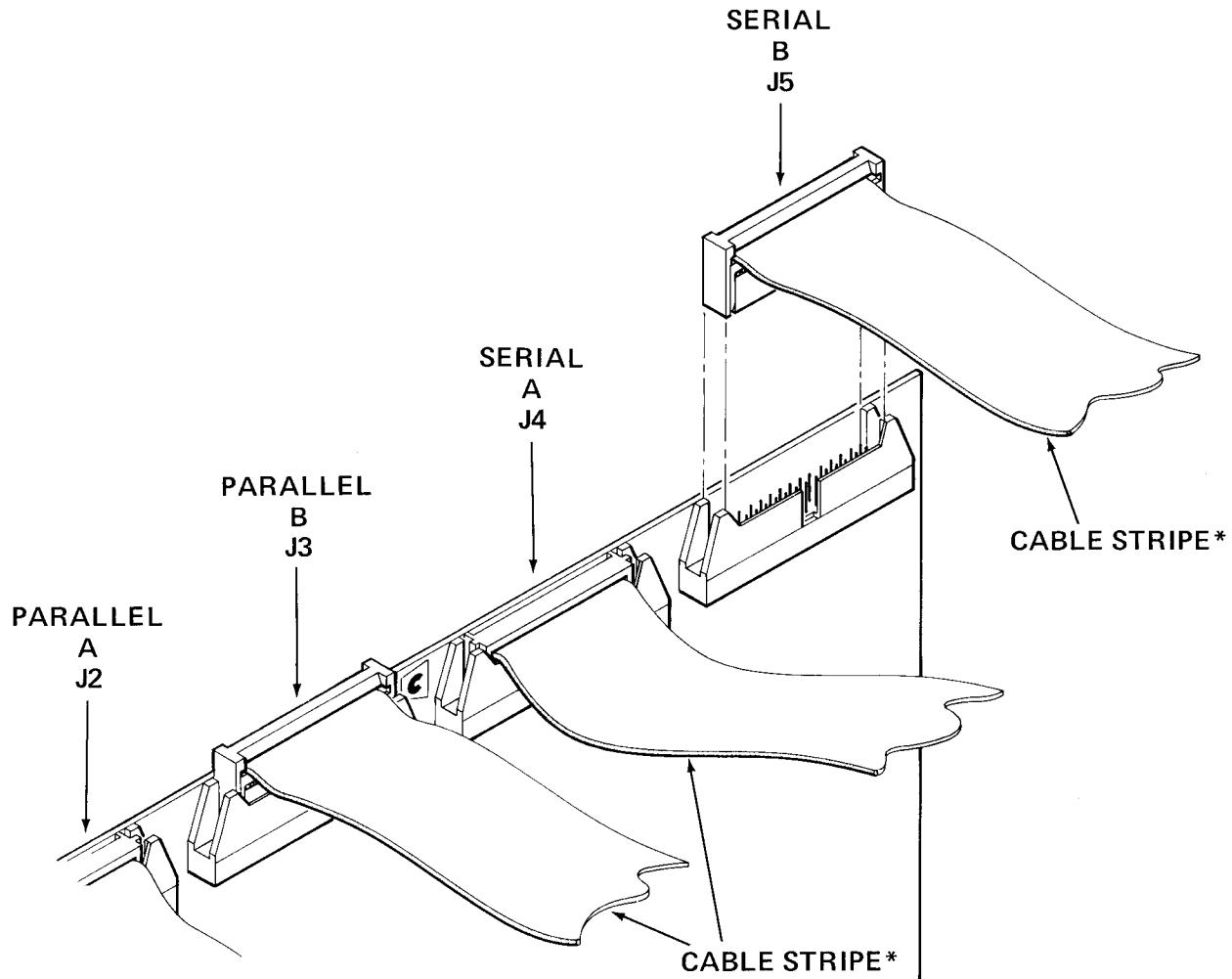
Figure 7 shows how flat wire cables should be connected to the TU-ART. Figure 8 shows a suggested wiring diagram.

Table 5 J4 Serial A

Pin	Name	Signal Direction	Voltage Level	Function
1	FRAME GROUND	---	---	Not connected on PC board. This pin should be tied to the chassis at the back panel if an RS232 terminal is being used.
2	INPUT A	Input	$\pm 12V$	RS232 data input.
3	OUT A	Output	$\pm 12V$	RS232 data output.
4	NC			
5	NC			
6	DSR	Output	+12V	RS232 data set ready. Tied to +12V through 1.5k (R5) on the PC board.
7	SIGNAL GND	---	0V	RS232 signal ground
8	CTS	Output	+12V	RS232 clear to send. Tied to +12V through 1.5k (R4) on PC board.
9-16	NC			
25	TTY PRINTER A (-)	Output	---	Data output current loop - (current sink)
23	TTY PRINTER A (+)	Output	+12V	Data output current loop + (current source)
17	TTY KEYBD A (+)	Input	+12V	Data input current loop + (current source)
24	TTY KEYBD A (-)	Input	-5V	Data input current loop - (current sink)
18-22	NC			
26	NC			

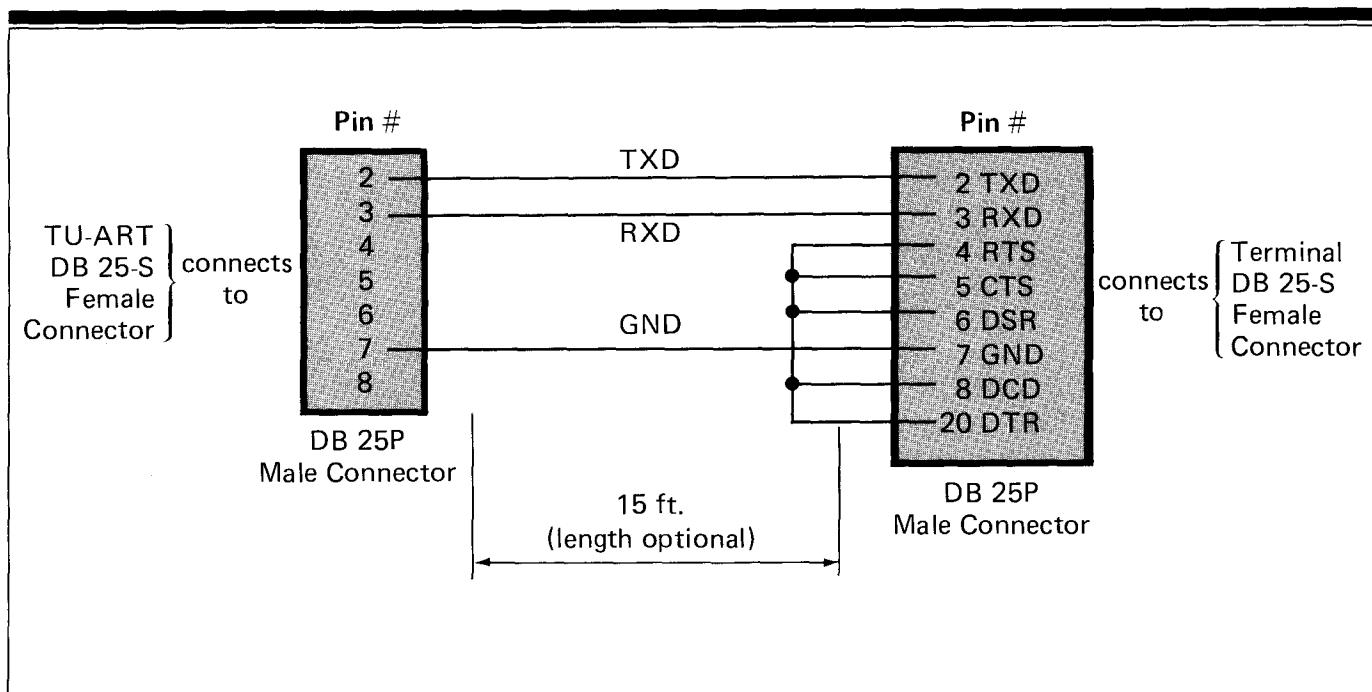
Table 6 J5 Serial B

Pin	Name	Signal Direction	Voltage Level	Function
1	FRAME GROUND	---	---	Not connected on PC board. This pin should be tied to the chassis at the back panel if an RS232 terminal is being used.
2	INPUT B	Input	$\pm 12V$	RS232 data input.
3	OUT B	Output	$\pm 12V$	RS232 data output.
4	NC			
5	NC			
6	DSR	Output	+12V	RS232 data set ready. Tied to +12V through 1.5k (R5) on PC board.
7	SIGNAL GND	---	$\emptyset V$	RS232 signal ground.
8	CTS	Output	+12V	RS232 clear to send. Tied to +12V through 1.5k (R4) on PC board.
9-16	NC			
25	TTY PRINTER B (-)	Output	---	Data output current loop - (current sink)
23	TTY PRINTER B (+)	Output	+12V	Data output current loop + (current source)
17	TTY KEYBD B (+)	Input	+12V	Data input current loop + (current source)
24	TTY KEYBD B (-)	Input	-5V	Data input current loop - (current sink)
18-22	NC			
26	NC			

Figure 7 Cable Connection

***NOTE:** Some ribbon cables may feed the female connector from the side opposite that illustrated in this figure. In all cases, the cable stripe must be aligned with the arrow head on the TU-Art legend.

Figure 8 Terminal To TU-ART Cable



This is a diagram of the cable required to connect a serial RS-232 I/O device (such as a CRT terminal) from the DB 25-S socket of the TU-ART cable (model TRT-CBL) to the DB 25-S connector of the RS-232 device.

The jumper connection between pins 4, 5, 6, 8 and 20 may not be required since some terminals have internal pullups on these lines.

4.3 Originate Mode Modification

The TU-ART board is factory wired in the **answer mode** for both serial I/O channels A and B. That is, serial data is input to the TU-ART at J4 or J5 pin 2 (RS232 IN) and serial data is output from the TU-ART over J4 or J5 pin 3 (RS232 OUT). In this context, the TU-ART is playing the role of the computer end of a serial line which is attached to a remote terminal.

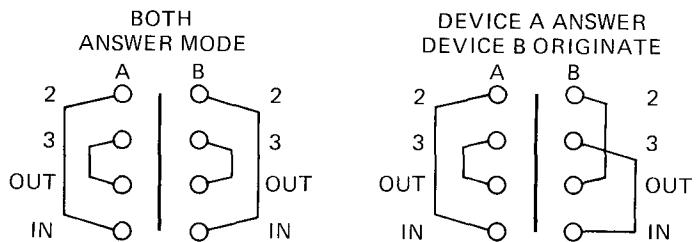
The TU-ART may be re-configured in the **originate mode** (that is, the TU-ART assumes the role of the remote terminal) by cutting foil traces and installing jumper wires as described below.

There are two vertical rows of pads located between connectors J4 and J5 (see illustration ahead). Device A and Device B may be independently configured in either the answer or originate modes.

To configure either device in the originate mode:

- 1) Cut the trace connecting the top and bottom pads on the appropriate device side (the trace connecting "2" and "IN").
- 2) Cut the trace connecting the middle two pads on the appropriate device side (the trace connecting "3" and "OUT").
- 3) Install an insulated jumper wire between pads "2" and "OUT."

- 4) Install an insulated jumper wire between pads "3" and "IN."



4.4 Spare RS232 Drivers And Receivers

There are two uncommitted sections in IC 9, a 75189 Receiver. Pads for jumper wires have been provided at pins 1, 2, 3 and at pins 11, 12, 13.

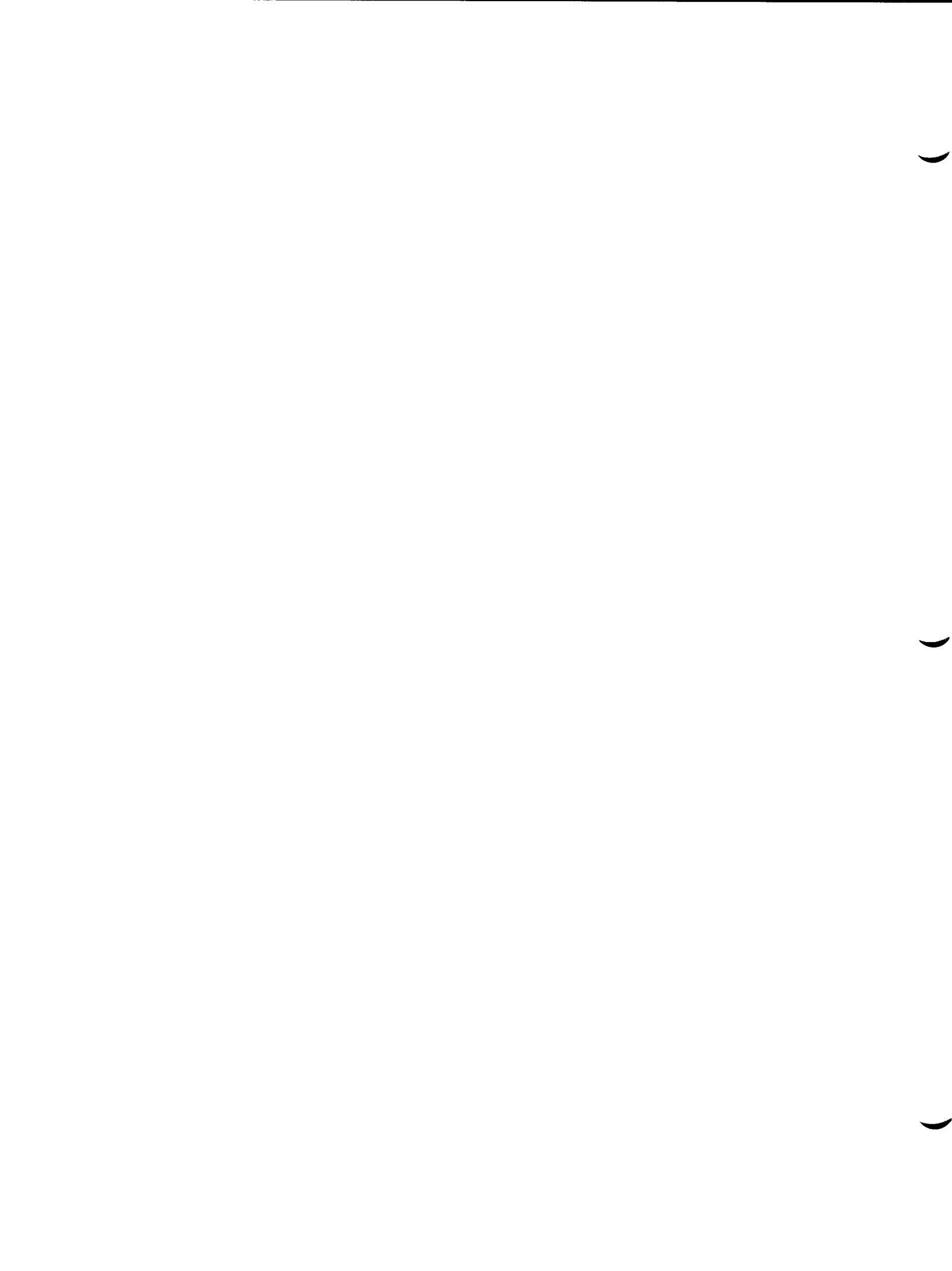
There are two uncommitted sections on IC 11, a 75188 driver. Pads have been provided at pins 4, 5, 6 and at pins 8, 9, 10.

These uncommitted sections are shown on the schematic diagram.

Section 5

Programming

Examples



Programming Examples

5.1 1-SEC Metronome

This program rings the console bell at 1-second intervals using Z80 mode interrupts. It is provided as an example of TU-ART operation. It is assumed that the CRT or terminal being used will be connected to serial

ports 0 and 1 of the 4FDC and that this program will be loaded and executed from the disk.

Set TU-ART switches 1, 6, 7, and 9 OFF; all other switches on the TU-ART DIP switch should remain ON. This addresses Device B at base port 50H and Device A at base port 80H. Note that Timer 1, Device A is used to generate the interrupt below.

```
0014 ;  
0015 ;  
0000 0016 ORG 100H  
0017 ;  
0100 F3 0018 TUART: DI  
0101 310003 0019 LD SP,300H  
0104 3E00 0020 LD A,0 ;Select Device A (see  
0106 D354 0021 OUT 54H,A ;software ADDR-REVERSE).  
0108 3E09 0022 LD A,9 ;Reset Device A & enable  
010A D382 0023 OUT 82H,A ;interrupt ack. response.  
010C 3E01 0024 LD A,1 ;Mask out all interrupts but  
010E D383 0025 OUT 83H,A ;those from Timer1, Device A  
0110 3E00 0026 LD A,0 ;Mask out all interrupts  
0112 D353 0027 OUT 53H,A ;from Device B.  
0114 3E02 0028 LD A,2 ;Select page 2  
0116 ED47 0029 LD I,A ;for interrupt vectors.  
0118 ED5E 0030 IM2 ;Interrupt mode 2 (Z80 mode).  
011A CD2801 0031 CALL INIT ;Initialize the Timer.  
0032 ;  
0033 ; What follows is an infinite loop. It could  
0034 ; instead be some useful program entirely  
0035 ; unrelated to the Timer program.  
0036 ;  
011D C31D01 0037 HERE: JP HERE  
0038 ;  
0039 ; Interrupt Service Routine.  
0040 ;  
0120 05 0041 TIMER: DEC B
```

5.2 Initialization Subroutine

```

0001 ;
0002 ;
0003 ; TUART PROGRAMMING EXAMPLES
0004 ;
0005 ;
0006 ;
(0000) 0007 ABASE: EQU 0 ;BASE ADDRESS DEVICE A
(0050) 0008 BBASE: EQU 50H ;BASE ADDRESS DEVICE B
0009 ;
(00C0) 0010 BAUDA: EQU 0C0H ;9600 BAUD,ONE STOP BIT
(0001) 0011 BAUDB: EQU 1 ;110 BAUD,TWO STOP BITS
(0000) 0012 ABDR: EQU ABASE ;BAUD RATE PORT A
(0050) 0013 BBDR: EQU BBASE ;BAUD RATE PORT B
0014 ;
(0009) 0015 RESET: EQU 9 ;RESET+INTA COMMAND
(0002) 0016 ACMD: EQU ABASE+2 ;COMMAND PORT A
(0052) 0017 BCMD: EQU BBASE+2 ;COMMAND PORT B
0018 ;
(0000) 0019 MASKA: EQU 0 ;NO INTERRUPTS FROM A
(0000) 0020 MASKB: EQU 0 ;NO INTERRUPTS FROM B
(0003) 0021 AMSK: EQU ABASE+3 ;INTERRUPT MASK PORT A
(0053) 0022 BMSK: EQU BBASE+3 ;INTERRUPT MASK PORT B
0024 ;
0025 ; EXAMPLE 1 -- INITIALIZATION ROUTINE
0026 ;
0027 ; SUBROUTINE INIT:
0028 ; CALLING PARAMETERS: NONE
0029 ; RETURN CONDITION: TUART INIT'ED
0030 ;
0031 ;
0000 0032 ORG 1000H
1000 F5 0033 INIT: PUSH AF ;SAVE STATE
1001 3E09 0034 LD A,RESET ;GET COMMAND
1003 D302 0035 OUT ACMD,A ;DEVICE A RESET
1005 D352 0036 OUT BCMD,A ;DEVICE B RESET
0037 ;
1007 3E00 0038 LD A,MASKA ;GET INTERRUPT MASK
1009 D303 0039 OUT AMSK,A ;MASK A SET
100B 3E00 0040 LD A,MASKB ;GET INTERRUPT MASK
100D D353 0041 OUT BMSK,A ;MASK B SET
0042 ;
100F 3EC0 0043 LD A,BAUDA ;GET BAUD RATE
1011 D300 0044 OUT ABDR,A ;RATE A SET
1013 3E01 0045 LD A,BAUDB ;GET BAUD RATE
1015 D350 0046 OUT BBDR,A ;RATE B SET
1017 F1 0047 POP AF ;RETRIEVE STATE
1018 C9 0048 RET

```

5.3 Character Output Subroutine

```
0050 ;  
0051 ; EXAMPLE 2 -- SUBROUTINE TO TRANSMIT A CHARACTER  
0052 ; TO DEVICE A  
0053 ;  
0054 ; SUBROUTINE CHAROUT:  
0055 ; CALLING PARAMETERS: ASCII CHR. IN REG. A  
0056 ; RETURN CONDITION:CHARACTER SENT  
0057 ;  
0058 ;  
(0000) 0059 ASTAT: EQU ABASE+0 ;STATUS REGISTER A  
(0001) 0060 ADATA: EQU ABASE+1 ;DATA REGISTER A  
(0080) 0061 TBE: EQU 80H ;BUFFER EMPTY BIT  
0062 ;  
1019 F5 0063 CHROUT: PUSH AF ;SAVE THE CHARACTER  
101A DB00 0064 SCHK: IN A,ASTAT ;READ STATUS  
101C E680 0065 AND TBE ;TRANSMIT BFR. EMPTY?  
101E 28FA 0066 JR Z,SCHK ;LOOP UNTIL READY  
1020 F1 0067 POP AF ;RETRIEVE CHARACTER  
1021 D301 0068 OUT ADATA,A ;TRANSMIT IT  
1023 C9 0069 RET ;DONE
```

5.4 Character Input Subroutine

```
0071 ;  
0072 ; EXAMPLE 3 -- SUBROUTINE TO READ A CHARACTER  
0073 ; FROM DEVICE A  
0074 ;  
0075 ; SUBROUTINE CHRIN:  
0076 ; CALLING PARAMETERS: NONE  
0077 ; RETURN CONDITION: ASCII CHR IN A  
0078 ; Z FLAG RESET  
0079 ;  
0080 ;  
(0040) 0081 RDA: EQU 40H ;DATA AVAILABLE BIT  
1024 DB00 0082 CHRIN: IN A,ASTAT ;GET STATUS  
1026 E640 0083 AND RDA ;RCVR DATA AVAIL?  
1028 28FA 0084 JR Z,CHRIN ;LOOP TILL READY  
102A DB01 0085 IN A,ADATA ;READ CHARACTER  
102C C9 0086 RET ;DONE
```

5.6 "Echo" Program

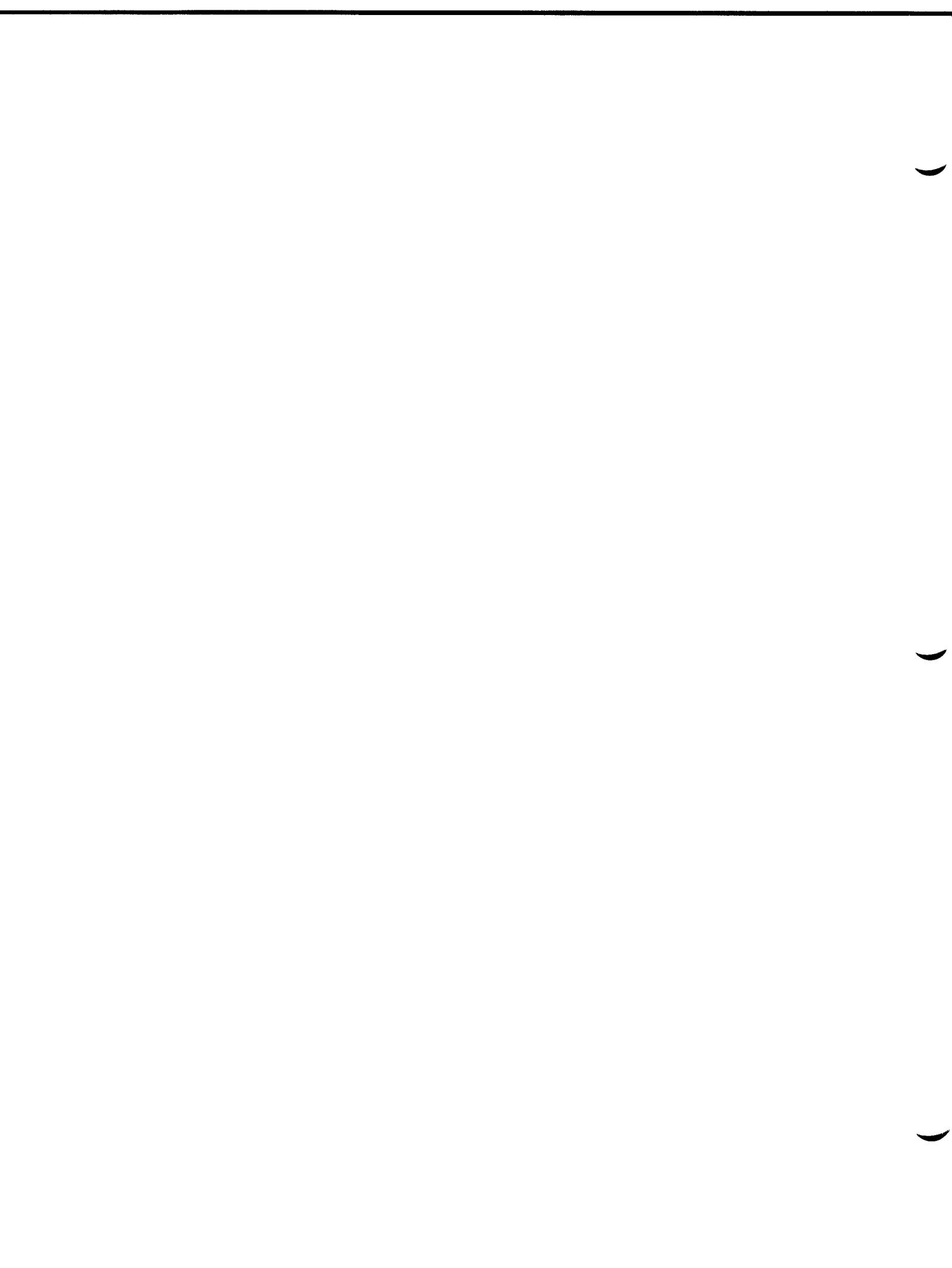
```
0088 ;           EXAMPLE 4 -- "ECHO" PROGRAM FOR DEVICE A
0089 ;  
0090 ;  
0091 ;  
102D      0092     ORG    100H  
          (0200) 0093 STACK: EQU    200H ;STACK AREA  
0100      310002 0094     LD     SP,STACK;SET STACK POINTER  
0103      CD0010 0095     CALL   INIT   ;RESET TUART  
0106      CD2410 0096 READ:  CALL   CHRIN  ;WAIT FOR AN INPUT  
0109      CD1910 0097     CALL   CHROUT ;NOW SEND IT BACK  
010C      18F8   0098     JR    READ   ;LOOP  
          0099 ;  
010E      (0000) 0100     END  
  
Errors      0
```

Section 6

TUART Kit

Assembly

Information



TU-ART Kit Assembly Information

If you purchased your TU-ART as a kit you will find the assembly to be straightforward. The locations of all the components are clearly marked on the pc board itself. Take care that the parts are positioned and oriented properly before they are soldered in place.

When installing the IC sockets note that no socket should be installed in the position marked "status socket." A socket is only used here if there is a need to change the assignment of status bits in the status word, as described on page 3 of this manual.

Also note that three different three-terminal regulators are used in the TU-ART: a 7805, 7812, and 7905.

These regulators are not interchangeable. Take caution that each regulator is installed in its proper position.

It is important that the "+" end of the tantalum capacitors are oriented as marked on the pc board. The cathode (banded) end of the 1N4742 diode (D1) must be oriented to the left. The flat surfaces of transistor Q1 and Q2 should also face the left.

After soldering all parts in place, install the ICs in their sockets. BE VERY CAREFUL THAT EACH PIN OF EVERY IC IS PROPERLY ENGAGED IN ITS SOCKET. After installing the ICs carefully, inspect your work.

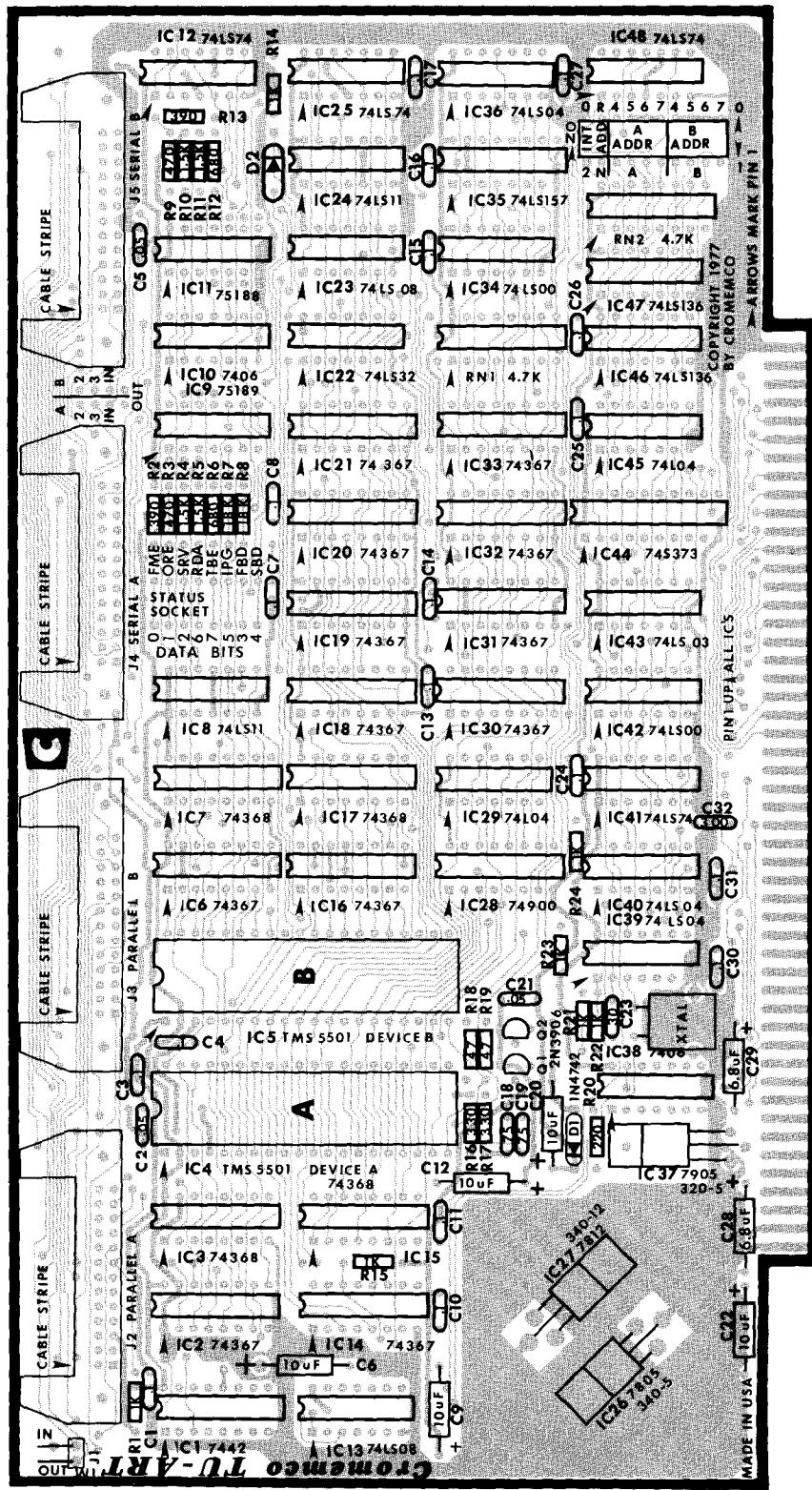
Parts List

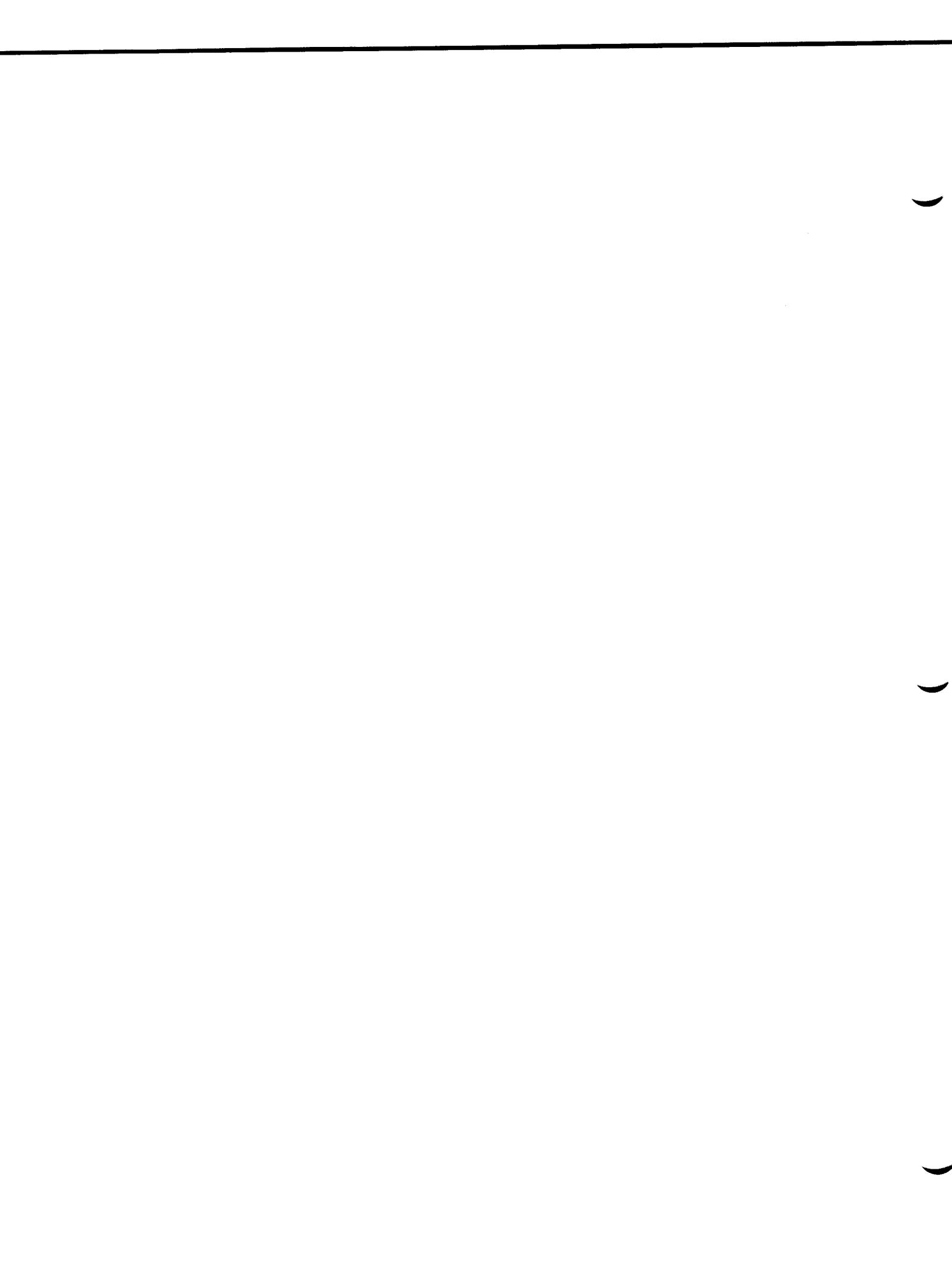
Integrated Circuits	Part No.	Integrated Circuits	Part No.
IC 1 7442	010-0022	IC 25 74LS74	010-0055
IC 2 74367	010-0080	IC 26 7805	012-0001
IC 3 74368	010-0079	IC 27 7812	012-0002
IC 4 5501	011-0005	IC 28 74900	010-0083
IC 5 5501	011-0005	IC 29 74L04	010-0074
IC 6 74367	010-0080	IC 30 74367	010-0080
IC 7 74368	010-0079	IC 31 74367	010-0080
IC 8 74LS11	010-0062	IC 32 74367	010-0080
IC 9 75189	010-0077	IC 33 74367	010-0080
IC 10 7406	010-0028	IC 34 74LS00	010-0069
IC 11 75188	010-0076	IC 35 74LS157	010-0046
IC 12 74LS74	010-0055	IC 36 74LS04	010-0066
IC 13 74LS08	010-0064	IC 37 7905	012-0000
IC 14 74367	010-0080	IC 38 7406	010-0028
IC 15 74368	010-0079	IC 39 74LS04	010-0066
IC 16 74367	010-0080	IC 40 74SL04	010-0066
IC 17 74368	010-0079	IC 41 74LS74	010-0055
IC 18 74367	010-0080	IC 42 74LS00	010-0069
IC 19 74367	010-0080	IC 43 74LS03	010-0067
IC 20 74367	010-0080	IC 44 74S373	010-0099
IC 21 74367	010-0080	IC 45 74L04	010-0074
IC 22 74LS32	010-0058	IC 46 74LS136	010-0050
IC 23 74LS08	010-0064	IC 47 74LS136	010-0050
IC 24 74LS11	010-0062	IC 48 74LS74	010-0055

Parts List

Capacitors	Part No.	Resistors	Part No.
C1 0.10 µF	004-0030	R1 1K	001-0018
C2 0.05 µF	004-0027	R2 390	001-0013
C3 0.10 µF	004-0030	R3 470	001-0014
C4 0.10 µF	004-0030	R4 1.5K	001-0020
C5 0.05 µF	004-0027	R5 1.5K	001-0020
C6 10.00 µF	004-0032	R6 680	001-0016
C7 0.10 µF	004-0030	R7 18K	001-0032
C8 0.10 µF	004-0030	R8 18K	001-0032
C9 10.00 µF	004-0032	R9 470	001-0014
C10 0.10 µF	004-0030	R10 1.5K	001-0020
C11 0.10 µF	004-0030	R11 1.5K	001-0020
C12 10.00 µF	004-0032	R12 680	001-0016
C13 0.10 µF	004-0030	R13 390	001-0013
C14 0.10 µF	004-0030	R14 1K	001-0018
C15 0.10 µF	004-0030	R15 1K	001-0018
C16 0.10 µF	004-0030	R16 330	001-0012
C17 0.10 µF	004-0030	R17 330	001-0012
C18 75.00 pF	004-0007	R18 47	001-0003
C19 75.00 pF	004-0007	R19 47	001-0003
C20 10.00 µF	004-0032	R20 220	001-0010
C21 0.05 µF	004-0027	R21 1K	001-0018
C22 10.00 µF	004-0032	R22 1K	001-0018
C23 30.00 pF	004-0003	R23 1K	001-0018
C24 0.10 µF	004-0030	R24 1K	001-0018
C25 0.10 µF	004-0030	RN1 4.7K DIP (15 resistors)	003-0017
C26 0.10 µF	004-0030	RN2 4.7K DIP (15 resistors)	003-0017
C27 0.10 µF	004-0030		
C28 6.80 µF	004-0034		
C29 6.80 µF	004-0034		
C30 0.10 µF	004-0030		
C31 0.10 µF	004-0030		
C32 300.00 pF	004-0015		
Miscellaneous	Part No.	IC Sockets	Part No.
1 Printed circuit board	020-0017	2 40 pin sockets	017-0006
1 10 pole DIP switch	013-0003	1 20 pin sockets	017-0004
4 26-pin cable sockets	017-0022	23 14 pin sockets	016-0001
1 Heatsink	021-0017	21 16 pin sockets	017-0002
Diodes/Transistors	Part No.		
D1 1N4742 Zener	008-0008		
D2 1N914	008-0002		
Q1 2N3906	009-0002		
Q2 2N3906	009-0002		

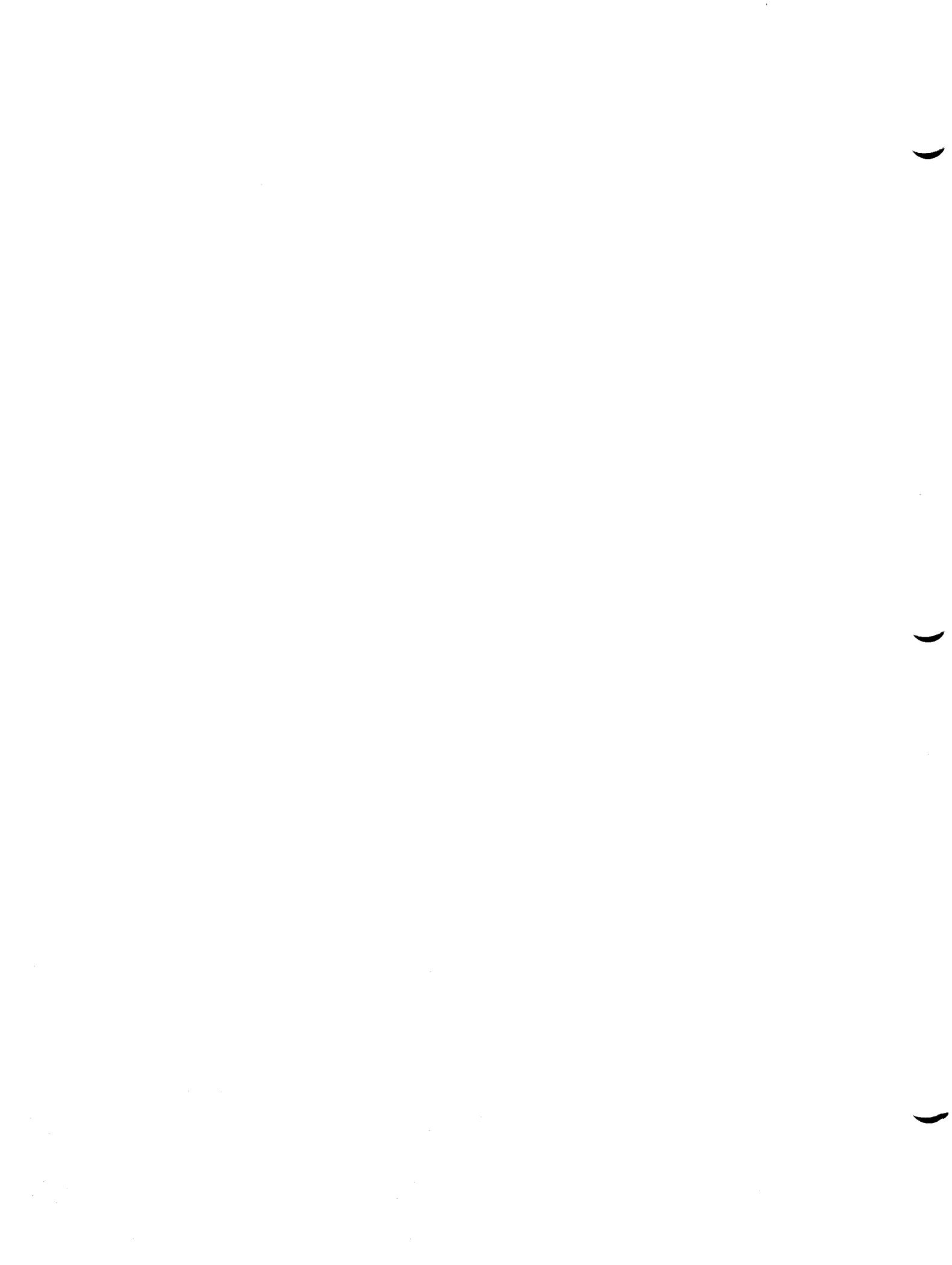
Parts Location Diagram





Section 7

Theory of Operation



Theory Of Operation

7.1 Introduction

The TU-ART has ten functional blocks supporting the TMS 5501s:

Power Supply Three IC regulators and a zener diode are used to generate ± 5 and ± 12 volts.

Crystal Controlled Clock An 8 MHz crystal oscillator is used as an on-board reference to control the internal state machine and to drive the $\emptyset 1$ and $\emptyset 2$ clocks of the TMS 5501s.

Address Select Two four-bit address comparators generate base address select signals when the four most significant device address bits of an input or output instruction agree with one of the two base address switch settings on the TU-ART. The base address select signals enable the appropriate TMS 5501 (depending on the current state of the Address Reverse multiplexer).

Function Decode The four function address pins on the TMS 5501s are driven by a read only memory addressed by the lower four bits of the S-100 address bus and status signal WO. The ROM also generates signals for internal bus control.

State Sequencer The internal state sequencer starts up whenever the TU-ART is addressed and cycles the internal bus through an 8080 M3-like sequence. The sequence starts with a SYNC pulse to the 5501s while the internal data bus is strobed with status information appropriate to the type of cycle requested by the processor (IO read, IO write, or Interrupt Acknowledge); continues while data is written or read; and terminates after signalling READY to the processor.

Status Strobe Data bus pins D \emptyset and D1 are controlled by the status strobe circuit during internal SYNC time to select the proper TMS 5501 operation.

Bus Multiplexers The internal data bus is time multiplexed (for status information), direction multiplexed (depending on the type of cycle: read or write), and path multiplexed (depending on the particular read-type function being performed) under control of the state generator and three-state bus drivers.

Serial Interface The TTL level serial output signal

from the TMS 5501s is converted to EIA RS/232 levels and to a teletype compatible current switch. Serial input may be from either EIA or teletype.

Parallel Interface TTL Bus buffers drive the parallel ports. Handshaking signals are controlled by the function decoder ROM.

Priority Chain A ripple priority resolver controls Data bit D \emptyset (INTA) on each TMS 5501 during SYNC time. This prevents both devices from responding to an Interrupt Acknowledge cycle from the processor when both devices have active interrupt requests. The priority chain is expandable to multiple boards.

These ten blocks, which are listed in the approximate order of attack for troubleshooting, will be discussed in detail below.

7.2 Power Supply

The TMS 5501s require three power supplies: $V_{CC} = +5$, $V_{DD} = +12$, and $V_{BB} = -5$. A -12V source is created by zener diode D1 for the EIA line driver and receiver IC's. The +12 supply is used by the EIA line drivers, the TTY interface, and the $\emptyset 1$, $\emptyset 2$ clock drivers. The -5 supply is used by the TTY interface.

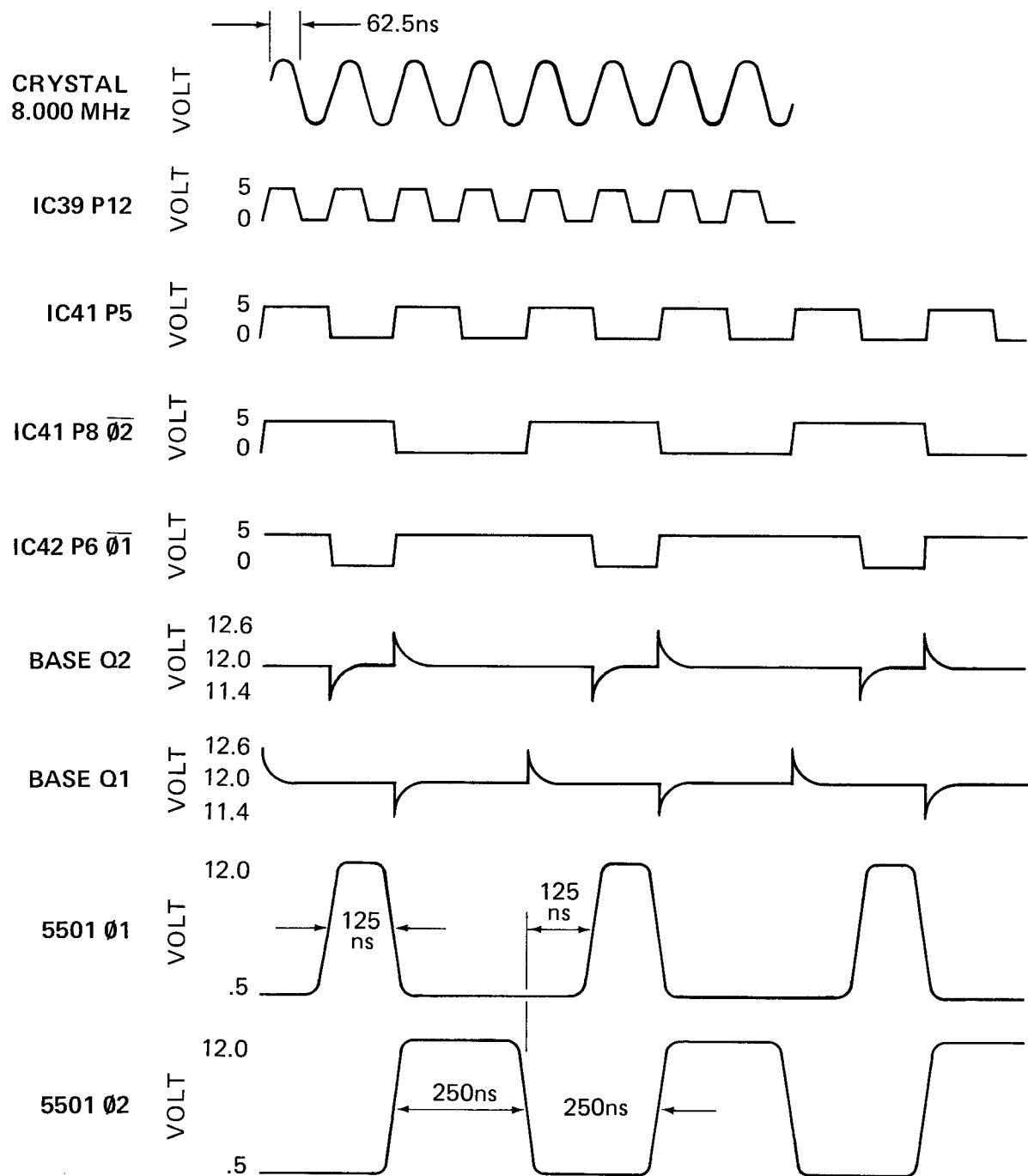
7.3 Crystal Controlled Clock

An 8.000 MHz crystal oscillator generates the TU-ART's timebase. A two-phase, 2MHz clock is derived from the IC41P8 ($\emptyset 2$ TTL) and IC42P6 ($\emptyset 1$ TTL). These signals are followed by high voltage inverters to generate the 12 volt clocks for the TMS 5501s. Transistors Q1 and Q2 form edge-active pullups for the inverters. A 75 pf - 330 ohm differentiator network on the base of each transistor couples a spike from the falling edge of the TTL input into the base. This switches the transistor on briefly and pulls the collector to +12 volts. A 47 ohm series resistor in the clock lead reduces ringing and overshoot. The rising edge of the TTL input turns on the 7406 inverter which pulls the collector of the transistor (now off) back to ground.

The state generator is clocked by $\emptyset 1$ TTL and $\emptyset 2$ TTL outputs from IC41P9 and IC41P8.

Clock waveforms are summarized in Figure 9.

Figure 9 Clock Waveforms



7.4 Address Select

Four-bit address comparison is performed by open collector exclusive or gates IC46 and IC47. Incoming address lines are deglitched and inverted by 74L04 inverters, then ex-ored with 4 bits from the DIP switch base address select positions. A closed switch matches a "1" on the Address bus; an open switch matches a "0" on the Address bus; when all four bits match and SOUT or SINP is active then the open collector wired — and node will go high. If the node at RN2P7 is high Base Address B is being selected. If RN2P5 is high Base Address A is being selected. When Device A is addressed IC43P6 pulls down the Device B select node to prevent bus conflict if both base addresses accidentally have been set equal. When either Device select is active IC40P10 goes low, enabling the Function Decoder ROM. Multiplexer IC35 performs Base Address reversing when its select pin goes low. In the normal case Device A select enables the CE driver of IC4, while Device B select enables the CE driver of IC5. Base address reversing enables IC5 in IC4's place and vice versa. The select pin of the MUX, IC35P1 is controlled by the signal applied to J2P1 or J3P1; or, if DIP Switch 2 is closed, by IC4P31 (the MSB of Device A's output parallel port).

7.5 Function Decode

TTL PROM IC28 is enabled when IC28P15 goes low (which occurs at the beginning of Input and Output cycles). IC28 is not enabled during interrupt acknowledge. When IC28 is enabled, it supplies function address signals to the 4 address pins of the 5501s. IC28P5 goes low during I/O operations involving the parallel ports and drives IC1, a decoder chip which generates Input and Output strobe signals. IC28P6 goes low during Output cycles. This signal controls the incoming bus buffers, generates a state-cycle request by pulling down IC24P10, and is strobed on the internal data bus bit D1 at SYNC time by IC43P3. IC28P7 goes low during INPUT cycles. This signal controls the outgoing bus drivers and generates a state-cycle request by pulling down IC24P9. This signal is not active (floats) during INTA cycles. IC28P9 goes low when the status port of the TMS 5501s is read. This signal controls an internal data path from the TMS 5501s to the output data latch, IC44.

7.6 State Sequencer

The heart of the TU-ART is the state sequencer, a four-stage shift register which times the status drivers and data in/out circuits to form an 8080-like internal

bus. The input to the state sequencer, IC25P2, is the signal from IC36P6 (IOREAD + IOWRITE + INTERRUPT ACKNOWLEDGE). While this signal is low, the state sequencer is held in a reset state by direct clear pins 1 and 13 of ICs 25 and 12. When the input goes high a high level will be shifted to IC25P5 at the first falling edge of $\emptyset 2$. IC23P8 then goes high, generating a SYNC signal at Pin 19 of both TMS 5501s and turning on status strobe driver IC18 through IC40P6 and IC43P1.

The state sequencer is now clocked by the rising edge of $\emptyset 2$, shifting a high level to IC25P9. IC23P10 goes low and remains low until the state sequencer is reset at the end of the I/O cycle. The status strobe drivers are shut off. The TMS 5501 now arranges internal data paths according to the address and status information it received during SYNC time. If the TU-ART is in an IOWRITE cycle the S-100 DO bus receivers IC18 and IC30 are enabled.

The state sequencer is clocked for a third time by $\emptyset 2$ falling edge, propagating the high level at IC25P9 to IC12P5. The Gate input of the DI bus latch is raised (IC44P11). The PRDY driver IC16 is disabled, signalling "READY" to the CPU, and releasing the bus from its WAIT condition.

The final change in state occurs on the rising edge of $\emptyset 2$ when IC12P8 goes low. This shuts off the DI latch gate. The state sequencer has completed its cycle and remains in this state until the processor terminates the I/O cycle.

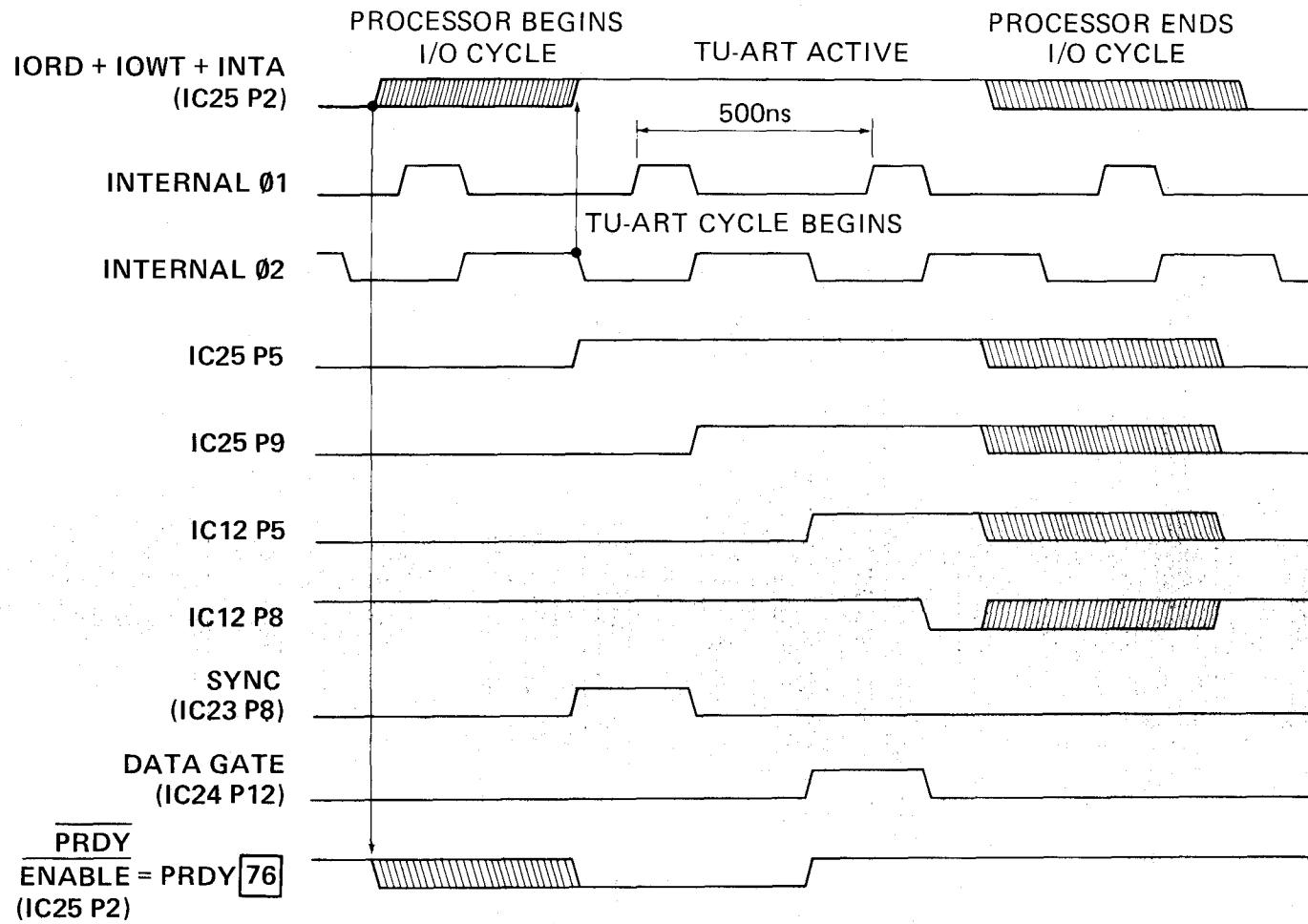
State sequencer timing is summarized in Figure 10.

7.7 Status Strobe

The TMS 5501s have no control pins for DBIN or WR; instead the ICs monitor bits D0 and D1 of the data bus during SYNC for status information. If D0 is high during SYNC, an Interrupt Acknowledge cycle is beginning, and the 5501 will send data to the bus during "T3" of the cycle. If D1 is high an IOREAD operation is beginning and the 5501 whose CE pin was high during SYNC will access the internal register addressed by A3-A0 and present data to the bus at "T3" of the cycle. If D1 is low during SYNC, an IOWRITE operation is beginning and the 5501 whose CE pin was high during SYNC will latch data from the bus during "T3" of the cycle.

Bit D1 is controlled by an open collector nand, IC 43, which is strobed by SYNC. Bit D0 is split into D0A and D0B so that INTA can be sent to the TMS 5501s individually. This is necessary because CE no longer selects the chip during interrupt acknowledge. Three-state driver IC18 controls D0A and D0B during SYNC.

Figure 10 State Sequencer Timing



7.8 Bus Multiplexers

The internal data bus which connects the two TMS 5501s will float while idle. At the beginning of a cycle it is strobed by the status drivers as described in the previous section. Following status the bus assumes one of five configurations (see Figure 11).

1. IOWRITE cycle: The S-100 DO bus receivers drive the internal data bus during $WR \cdot (T \geq T_2)$.
2. IOREAD (EXCEPT READ STATUS PORT): The internal data bus is buffered by a set of permanently-enabled 74367 sections, then passed through another set of 74367s, enabled by the assertion of READ and STATUS. These 74367s drive the output latch IC44 which latches during T3 of the internal cycle. IC44 has three state output drivers built in which drive the S-100 D1 bus during $DBIN \cdot IOACTIVITY$.
3. IOREAD STATUS: The buffered internal data bus passes through the status bit select pocket where bits from the 5501 may be arranged arbitrarily in order to control flag bit assignments. The "scrambled" bits are then passed through 74367s which have been enabled by STATUS going low. The output latch operates as before.
4. INTA MODE 0 (8080): During MODE 0 INTA the buffered internal data bus bits D3-D5 are routed through 74367s straight to the output latch. The remaining bits are passively pulled high.
5. INTA Mode 2 (Z-80): During a mode 2 INTA the buffered internal data bus bits D3-D5 plus INTA B plus A7, A6 and A5 from Base address A form inputs to a set of 74367s which drive the output latch.

7.9 Serial Interface

Transmit output from the TMS 5501 is inverted to RS232 levels by IC11 (1488). Output is also provided

from a 7406 high voltage inverter for grounding a 20 mA current source or for TTL level output. The RS232 output idles at -12v, the 7406 output idles at ground (conducting).

Receiver input is taken from an RS232 line receiver, IC9 (1489). IC9 converts RS232 levels to TTL. When a TTY keyboard is used, it switches the bias voltage on IC9 from +12 to -5 which causes TTL level switching at the output.

The output of the 1489 idles at +5 volts.

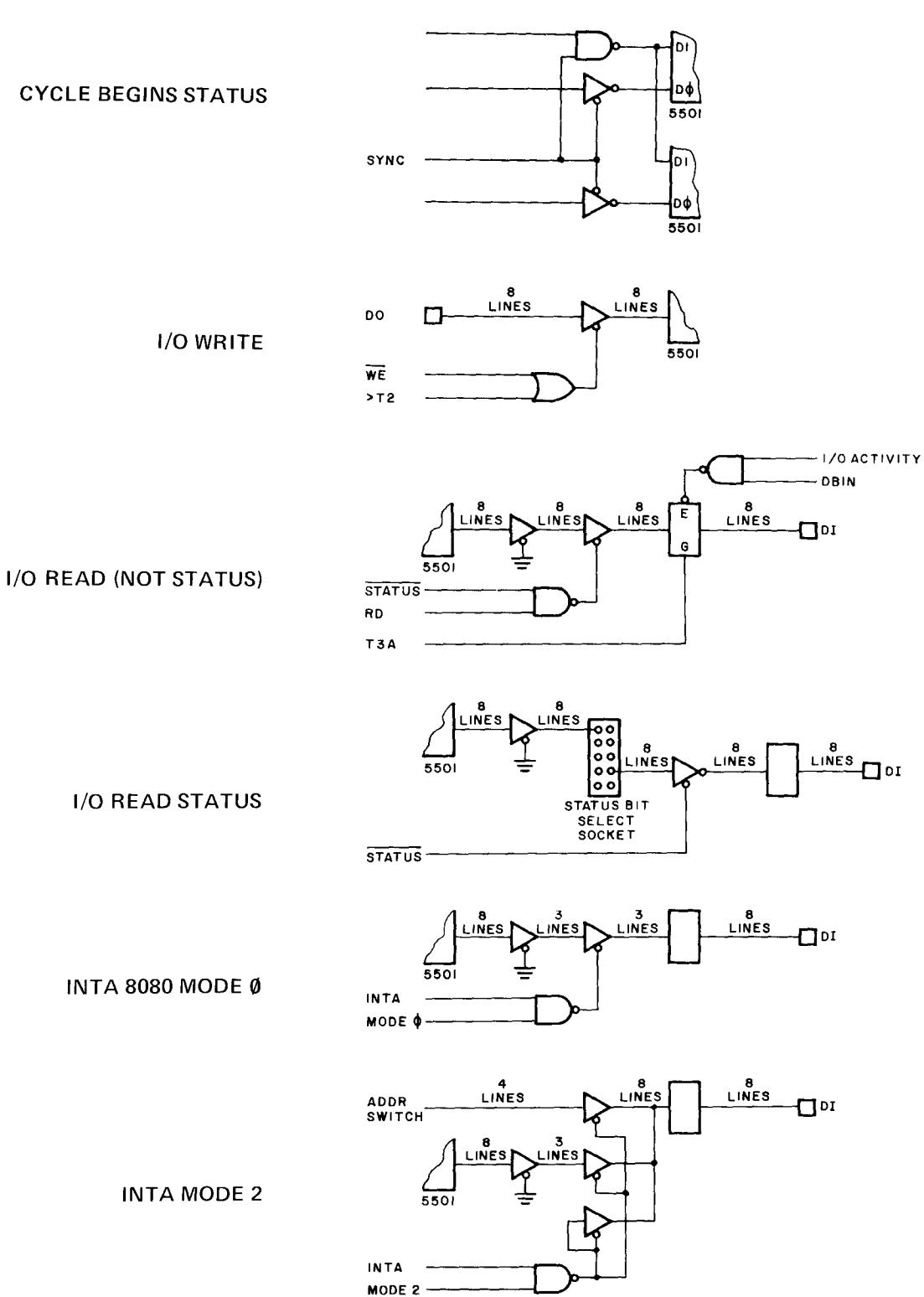
7.10 Parallel Interface

Parallel inputs to the TMS 5501 are TTL buffered by 74367s. Parallel outputs are inverted and buffered by 74368s to keep positive logic. The 74368s may be three stated by grounding DISABLE. Strobe signals are decoded by IC1.

7.11 Priority Chain

The TU-ART will respond to an Interrupt Acknowledge cycle from the processor when three conditions are satisfied: 1) The processor has raised SINTA, the Interrupt Acknowledge status signal, 2) one of the TMS 5501s is requesting interrupt (high level on IC4P23 or IC5P23), and 3) no other device higher up the priority chain is requesting an interrupt. The priority chain input at J1 is used to clear IC48, the INTA enable flip flop. Suppose IC4 (Device A) requested an interrupt at the same time as IC5 (Device B). If Priority IN was being held low by a higher priority TU-ART, both sections of IC48 would remain cleared, disabling IC23P5 and IC23P6 from generating SINTA status bits. When Priority IN is allowed to float to +5, the next M1 occurrence will clock the two sections of IC48 (M1 may be the start of an INTA cycle, though it doesn't have to be). Both IC48P5 and IC48P9 go high momentarily because both DEVICE A and Device B have interrupts pending. However IC48P6 ripples through IC13P3 to force IC48P9 low in exactly the same manner as PRIORITY IN from J1. Thus only DEVICE A actually receives the INTA status bit and no bus conflict is allowed.

Figure 11 Bus Signal Flow



Application Notes

8.1 Cromemco TU-ART Interface For The Oliver Audio Engineering Mode OP-80A Paper Tape Reader (or any device requiring a parallel port with hand shake)

This routine uses the TU-ART Sense line as a DATA READY flag for the parallel port:

0000: F3	DI	DISABLE INTERRUPTS
0001: 3E 04	MVI A,04H	GET INT. MASK FOR SENS
0003: D3 03	OUT 03	OUTPUT IT
0005: DB 00	IN 00	GET STATUS
0007: E6 20	ANI 20	ISOLATE INT. PENDING BIT
0009: CA 01 00	JZ 0001H	WAIT FOR NEW DATA
000C: DB 03	IN 03	CLEAR CAUSE OF INT.
000E: DB 04	IN 04	GET DATA FROM PARALLEL PORT & GENERATE NACK

*User routine
goes here.
Example:*

0010: CD 12 E1	CALL PCHR	PRINT ASCII CHAR.
0013: C3 00 00	JMP 0000H	DO AGAIN

CONNECT RDA TO SENSA LINE (J2 Pin 15)

CONNECT INPSTBA (J2 Pin 2) TO NACK

CONNECT THE EIGHT DATA LINES TO INPUT BITS 0-7 ON J2 (Pins 4-7 and 10-13)

CONNECT GND TO SIGNAL GND (J2 Pin 14)

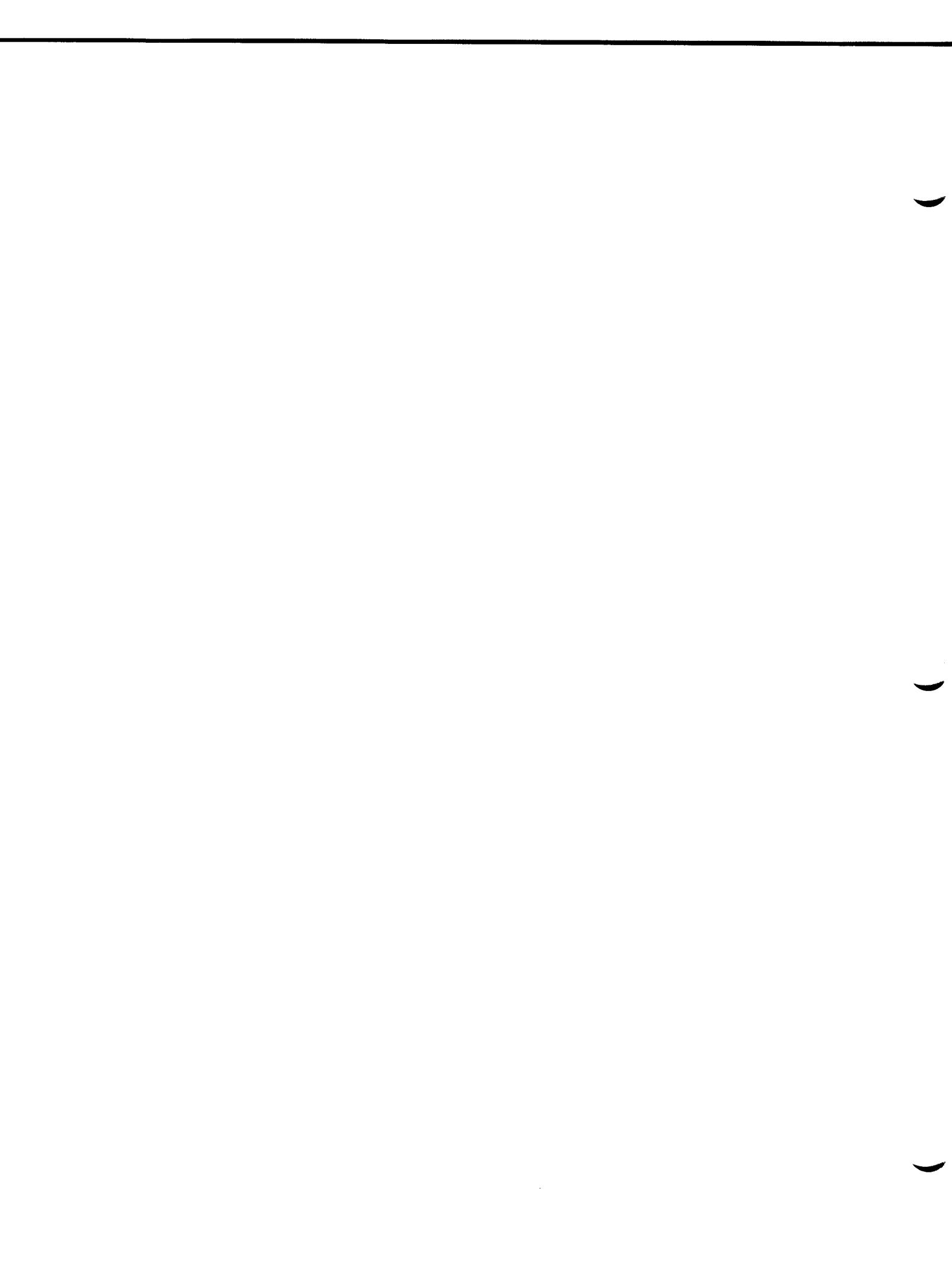
CONNECT +5V TO VCC (Pin 3)

8.2 Using The TU-ART In 4FDC Systems

The TU-ART is often used to provide additional I/O facilities in systems based around the Cromemco 4FDC Disk Controller. Since the 4FDC has a built-in I/O port which is addressed at 00H (base address), the TU-ART

will conflict if the usual addresses of 00H and 50H are used. We recommend 20H and 80H for Device A base address and Device B base address, respectively.

If CDOS is used, the TU-ART will be initialized for you. If CDOS is not used you must be certain to initialize both sections of the TU-ART (even if only one section is used) to prevent spurious interrupts.



Section 8

Application Notes



ASCII Character Codes

DEC	CHAR	DEC	CHAR	DEC	CHAR	DEC	CHAR
000	CTRL-@	033	!	066	B	099	c
001	CTRL-A	034	"	067	C	100	d
002	CTRL-B			068	D	101	e
003	CTRL-C	035	#	069	E	102	f
004	CTRL-D	036	\$	070	F	103	g
		037	%	071	G	104	h
005	CTRL-E	038	&	072	H		
006	CTRL-F	039	'	073	I	105	i
007	CTRL-G			074	J	106	j
008	BS	040	(075	K	107	k
009	HOR. TAB	041)	076	L	108	l
		042	*	077	M	109	m
010	LINE FEED	043	+	078	N	110	n
011	VERT. TAB	044	,	079	O	111	o
012	FF			080	P	112	p
013	CR	045	-	081	Q	113	q
014	CTRL-N	046	.	082	R	114	r
		047	/	083	S	115	s
015	CTRL-O	048	Ø	084	T	116	t
016	CTRL-P	049	1	085	U	117	u
017	CTRL-Q			086	V	118	v
018	CTRL-R	050	2	087	W	119	w
019	CTRL-S	051	3	088	X	120	x
		052	4	089	Y	121	y
020	CTRL-T	053	5	090	Z	122	z
021	CTRL-U	054	6	091	[123	{
022	CTRL-V			092	\	124	
023	CTRL-W	055	7	093]	125	}
024	CTRL-X	056	8	094	↑	126	-
		057	9	095	—	127	DEL
025	CTRL-Y	058	:				
026	CTRL-Z	059	;				
027	CTRL-[
028	CTRL-\	060	<				
029	CTRL-]	061	=				
		062	>				
030	CTRL-↑	063	?	096	,		
031	CTRL_-	064	@	097	a		
032	SPACE	065	A	098	b		

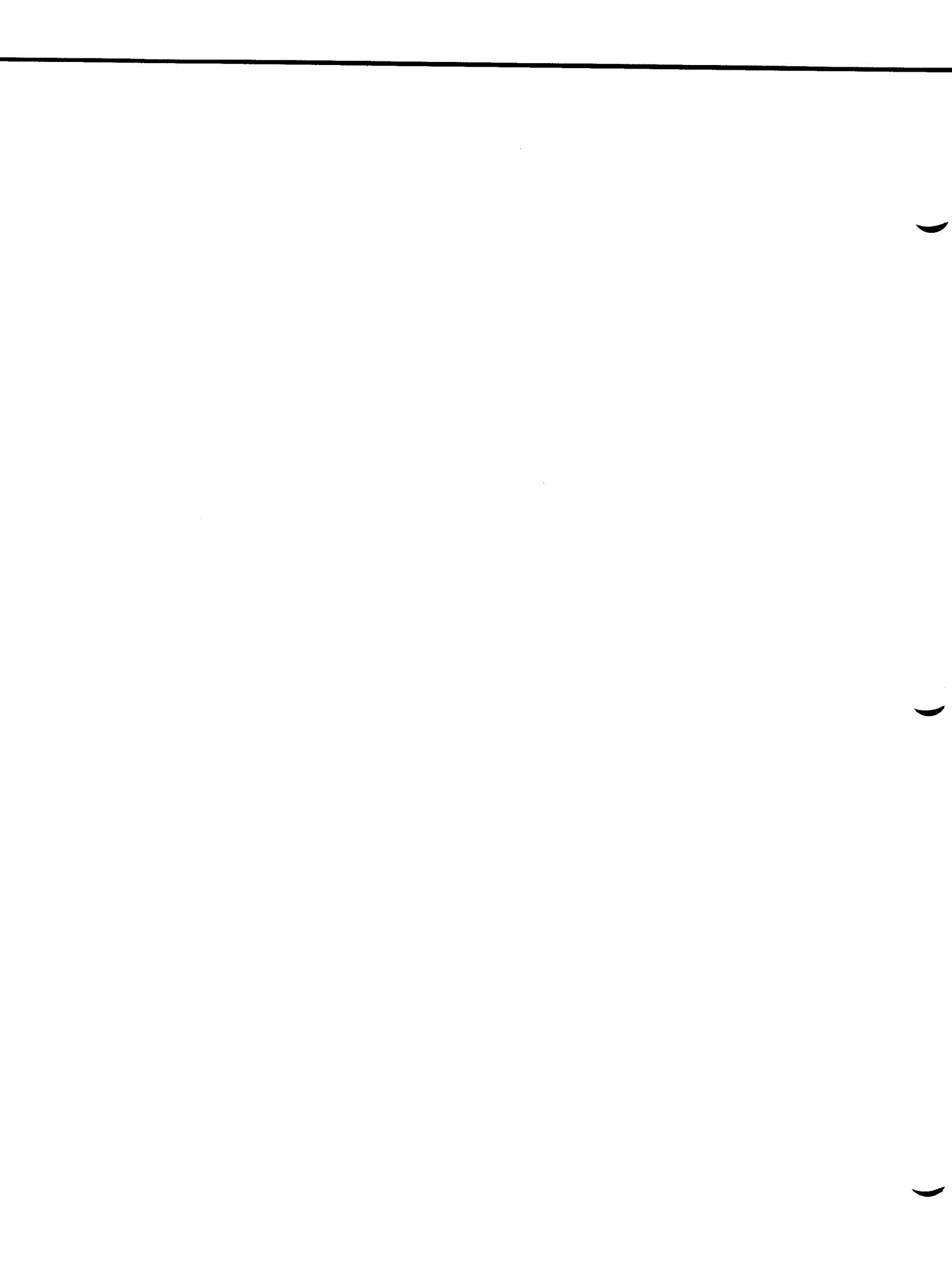
CTRL = Control Character

BS = Backspace

CR = Carriage Return

FF = Form Feed

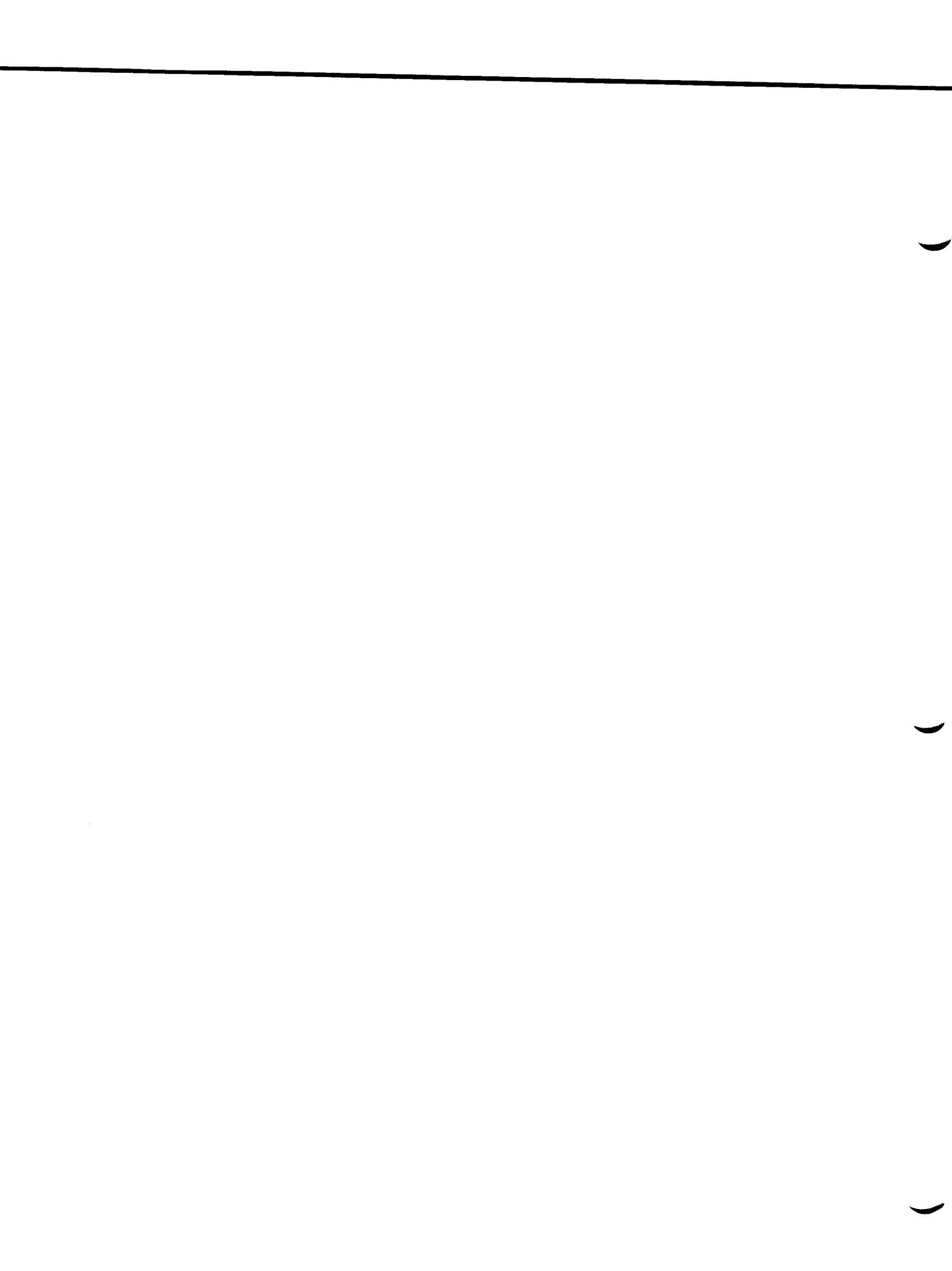
DEL = Rubout

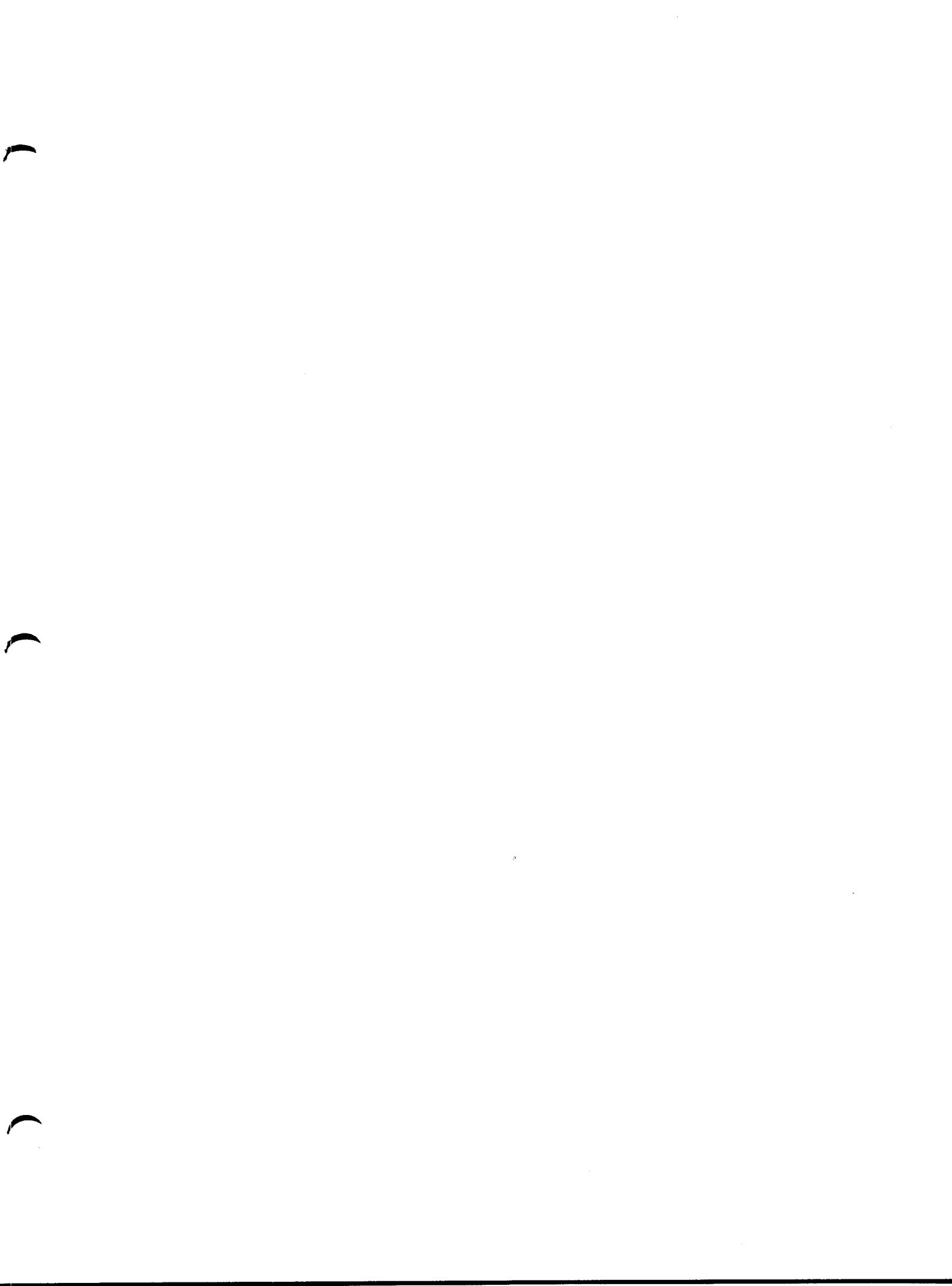


Limited Warranty

Cromemco, Inc. warrants this TU-ART Digital Interface board against defects in materials and workmanship for a period of Ninety (90) days from the date of delivery to the customer. Cromemco, Inc. will replace or repair at its option this product should it prove to be defective due to defects in materials or workmanship during the warranty period, provided that this product is returned to Cromemco, Inc. postage or shipping prepaid and adequately packaged for shipment to insure against loss. If this product fails after the above Ninety (90) day warranty period, it will be repaired for a fixed prepaid service fee provided that this product is returned to Cromemco, Inc. postage or shipping prepaid and adequately packaged for shipment to insure against loss. Cromemco, Inc. reserves the right to refuse to repair any product that in the discretion of Cromemco, Inc. has been subjected to electrical or mechanical abuse or not handled with reasonable care. The service fee is currently \$70 and is subject to change without notice.

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